Обещающая компиляция в ARMv8

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Что нужно для быстрого ПО?

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$$[x] := 1;$$
$$a := [y]$$

Компилятор:
Независимые обращения.
Можно переупорядочить.

$$[x] := 1;$$
$$a := [y]$$

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Процессор:

Независимые обращения.

Можно выполнить не по порядку.

$$[x] := 1;$$
$$a := [y]$$

Всегда ли корректны такие преобразования?

$$[x] := 1;$$
$$a := [y]$$

$$
\begin{array}{c}
[x] := 0; [y] := 0 \\
[x] := 1; \parallel [y] := 1; \\
a := [y] \parallel b := [x]
\end{array}
$$

$$
\begin{array}{c|c|c}
[x] := 0; [y] := 0 & & \\
\hline
[x] := 1; & \| & [y] := 1; \\
a := [y] & \| & b := [x]
\end{array}
$$

$$a = b = 0$$

$$[x] := 0; [y] := 0$$

A если переупорядочить?

$$a = b = 0$$

$$
\begin{array}{l}
[x] := 0; [y] := 0 \\
\left(\begin{array}{l|l}
[x] := 1; & [y] := 1; \\
a := [y] & b := [x]
\end{array}\right)
\end{array}
$$

$$a = b = 0$$

$$
\begin{array}{c||c}
[x] := 0; [y] := 0 & \\
a := [y]; & [y] := 1; \\
[x] := 1 & b := [x]
\end{array}
$$

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\begin{array}{c|c}
[x] := 0; [y] := 0 & \\
a := [y]; & [y] := 1; \\
[x] := 1 & b := [x]
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\begin{array}{r}
[x] := 0; [y] := 0 \\
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$$a = b = 0$$

$$[x] := 0; [y] := 0$$

$$\left(\begin{array}{l|l} [x] := 1; & [y] := 1; \\ a := [y] & b := [x] \end{array}\right.$$

$$a = b = 0$$

Такое поведение наблюдается в реальности (например, GCC + x86)!

Модели памяти процессоров

Модели памяти ЯП

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- Power, [Alglave et al., 2014]
- ARM, [Flur et al., 2016]
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Имеют ряд существенных недостатков

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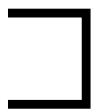

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Корректность компиляции показана в [Kang et al., 2017]

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Та же схема доказательства не подходит для ARM!

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Результаты данной работы

- Доказана корректность компиляции подмножества “обещающей” семантики [Kang et al., 2017] в модель ARMv8 [Flur et al., 2016]

Результаты данной работы

- Доказана корректность компиляции подмножества “обещающей” семантики [Kang et al., 2017] в моде

Расслабленные (relaxed) чтения и записи, высвобождающие (release) и преобретающие (acquire) барьеры памяти

Результаты данной работы

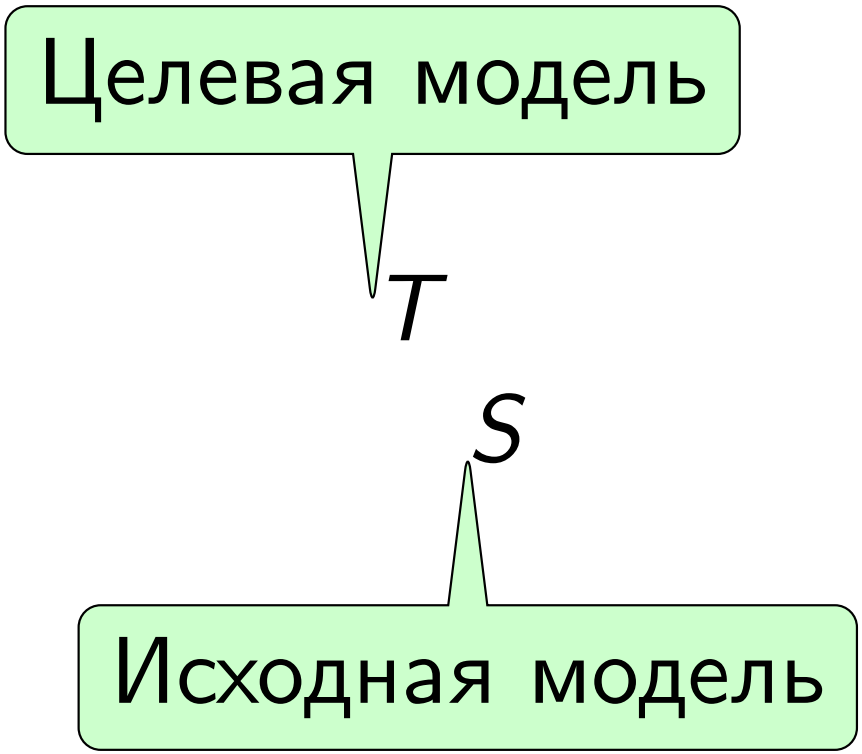
- Доказана корректность компиляции подмножества “обещающей” семантики [Kang et al., 2017] в модель ARMv8 [Flur et al., 2016]

- Формализована модель ARMv8 [Flur et al., 2016] и доказаны вспомогательные утверждения про неё

Корректность компиляции...

Корректность компиляции... Что это значит?

Корректность компиляции из S в T



Корректность компиляции из S в T

Исходная программа

$\forall Prog \in Syntax,$

T

$compile(Prog)$

S

Результат компиляции

Корректность компиляции из S в T

$$\forall Prog \in Syntax,$$
$$\{t_j\}_{j\in[1..k]} \underset{S}{-} T\text{-исполнение } compile(Prog).$$

Корректность компиляции из S в T

$\forall Prog \in Syntax,$

$\{t_j\}_{j \in [1..k]}$ – T-исполнение $compile(Prog)$.

$\exists \{s_i\}_{i \in [1..n]}$ – S-исполнение $Prog$,

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$s_n \simeq t_k$.

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e.g., финальное состояние памяти совпадает

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Рассматриваем $compile = id$

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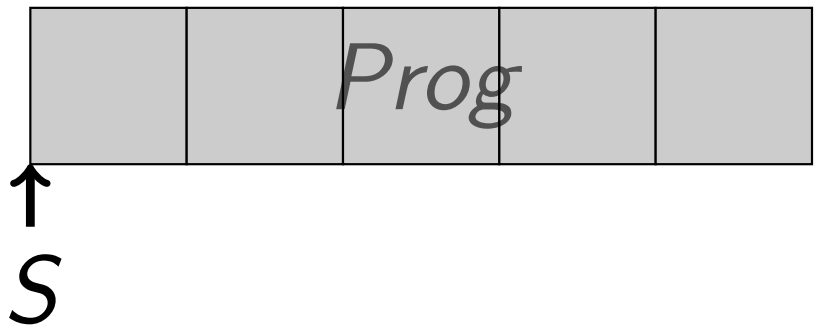
Стандартная техника — симуляция

Пример симуляции



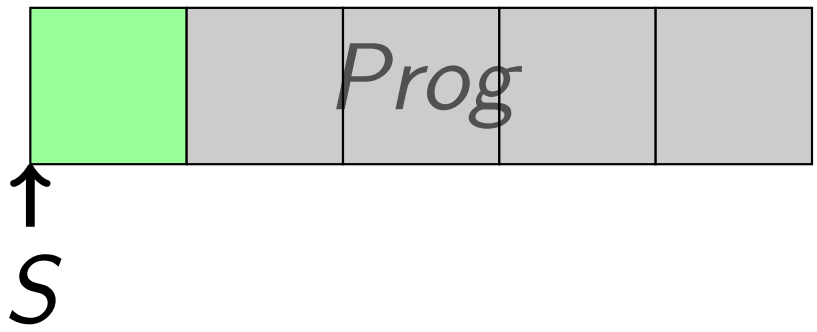
Инвариант выполняется

– выполнено T

S – исходная модель

T – целевая модель

Пример симуляции



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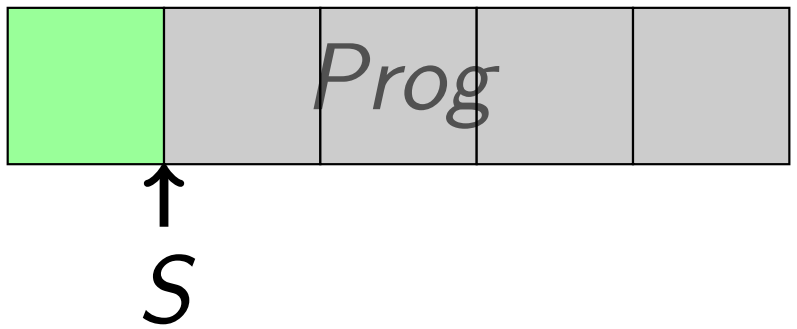

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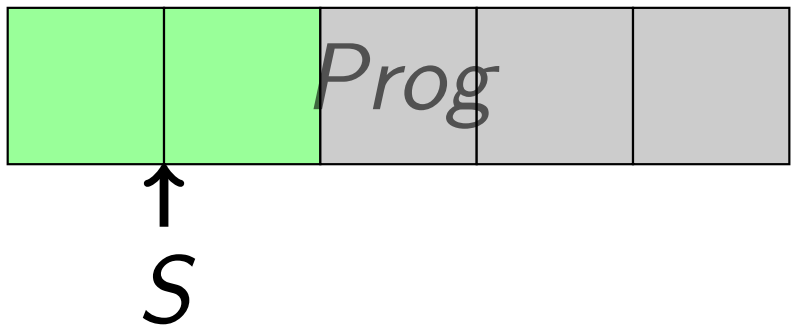

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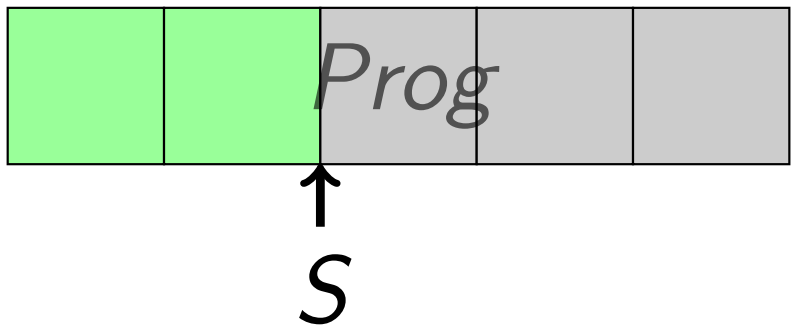

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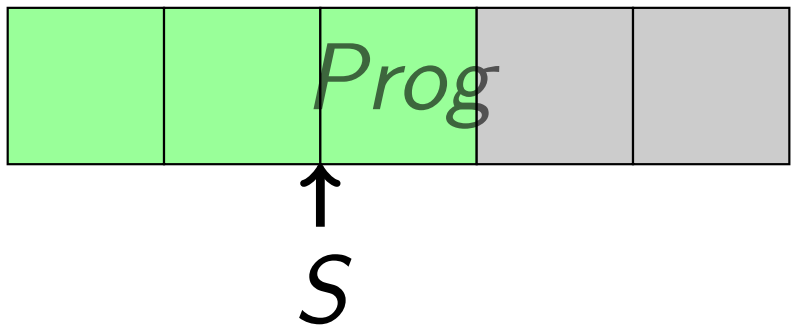

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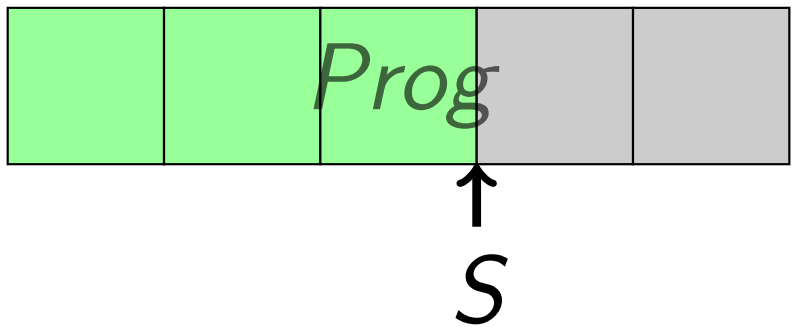

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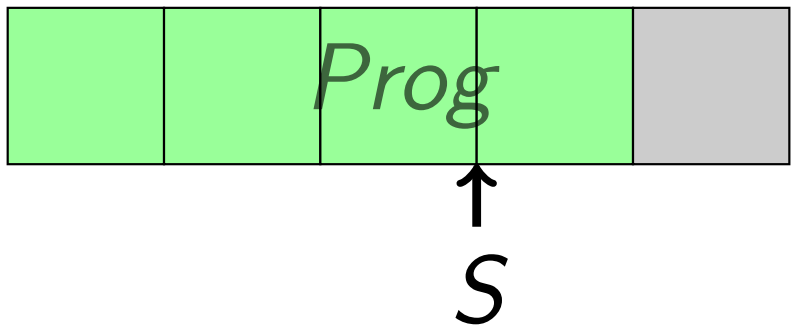

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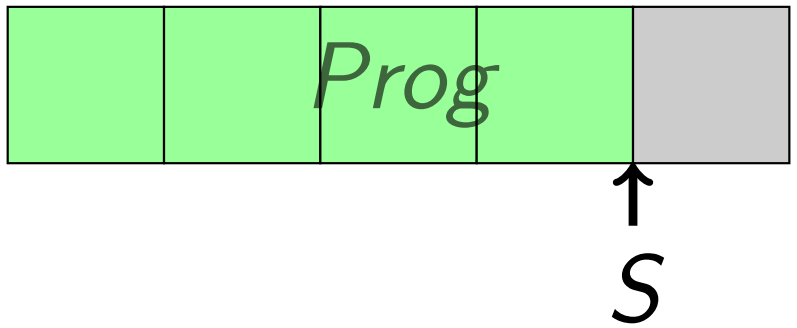

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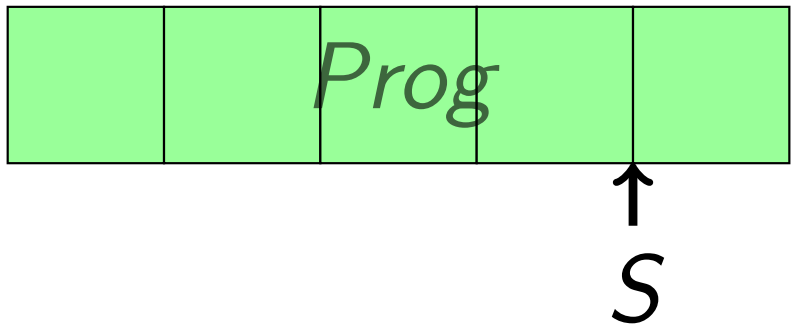

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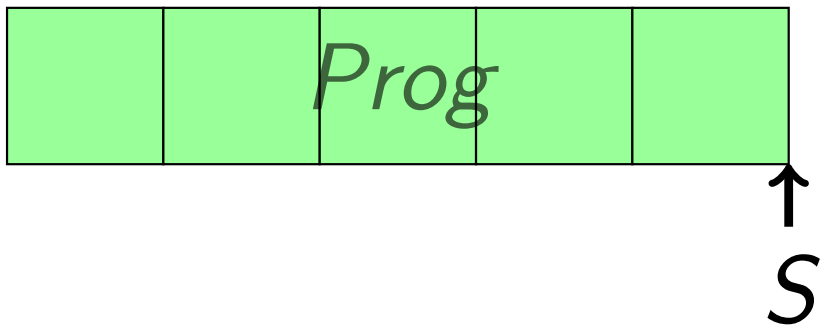

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...но симуляция напрямую не применина в нашем случае

...но симуляция напрямую не применина в нашем случае:

1. ARM выполняет инструкции не по порядку;
2. “Обещающая” семантика имеет больше явных ограничений.

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1. Вводим промежуточную семантику ARM+τ

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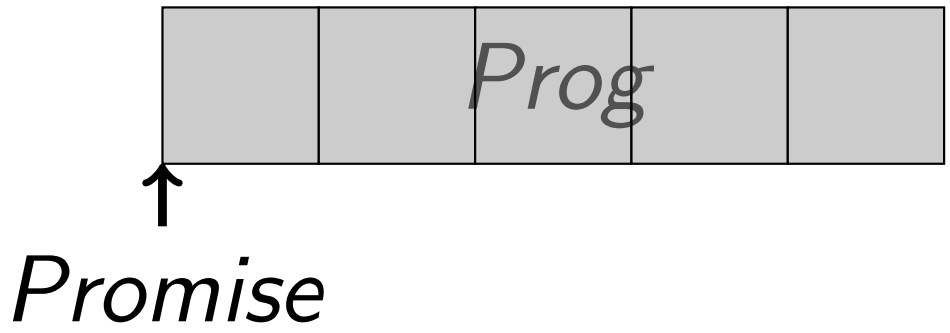
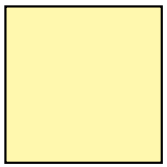
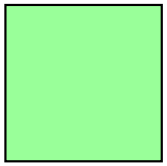
“Запаздывающая” симуляция



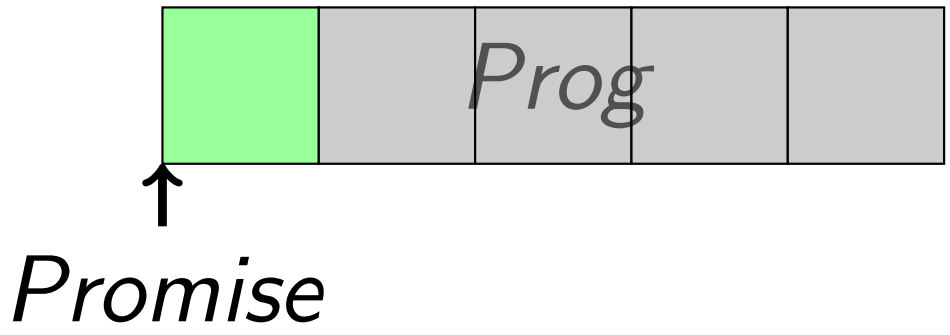
Инвариант: “обещающая” машина ждёт

 – частично выполнено *ARMv8*

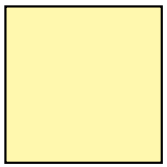
 – выполнено *ARMv8*

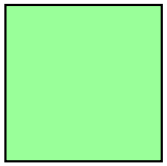
Promise – “обещающая” модель

“Запаздывающая” симуляция



Инвариант: “обещающая” машина исполняется

 – частично выполнено *ARMv8*

 – выполнено *ARMv8*

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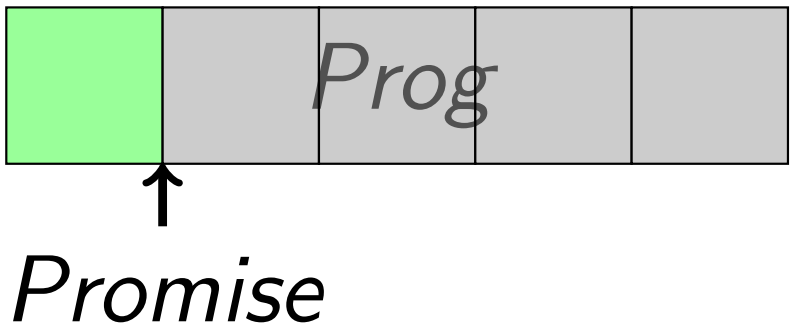

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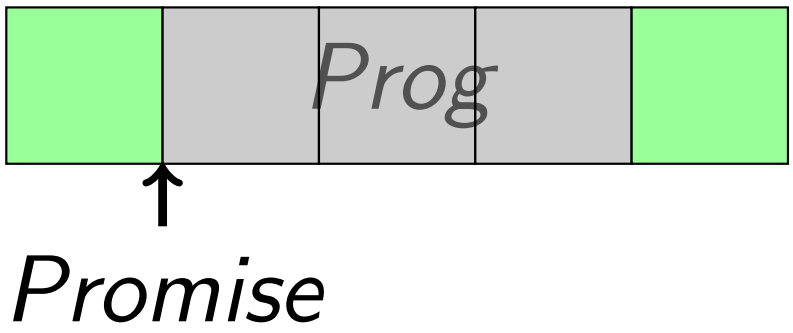
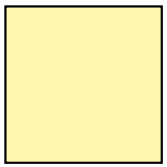
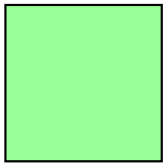


Инвариант: “обещающая” машина ждёт

 – частично выполнено *ARMv8*

 – выполнено *ARMv8*

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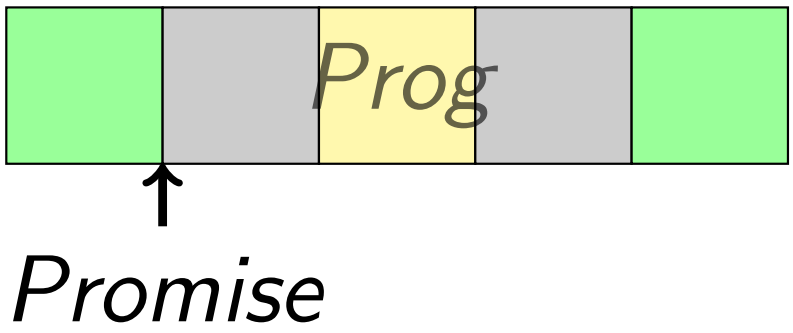
“Запаздывающая” симуляция



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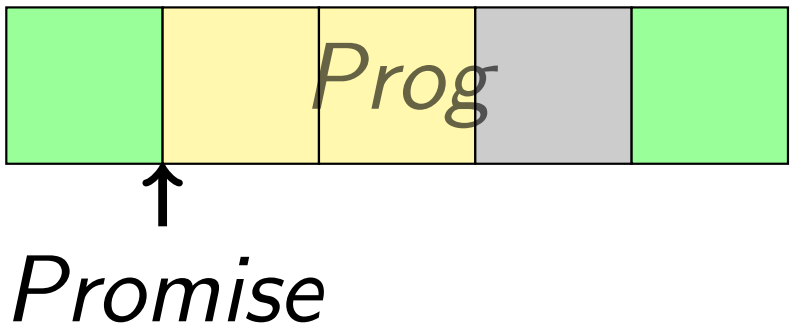

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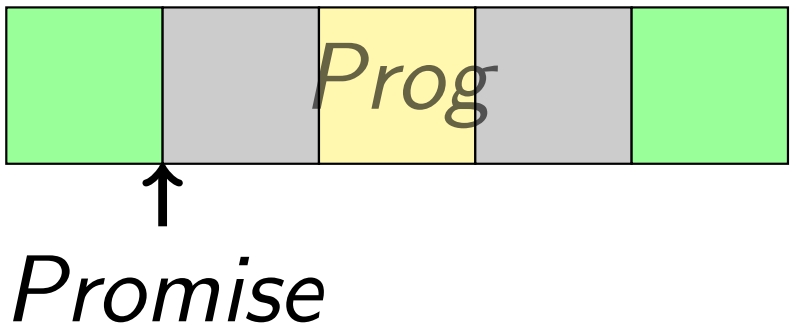

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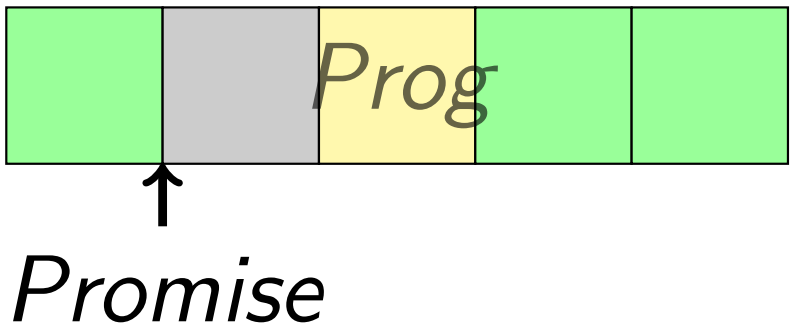

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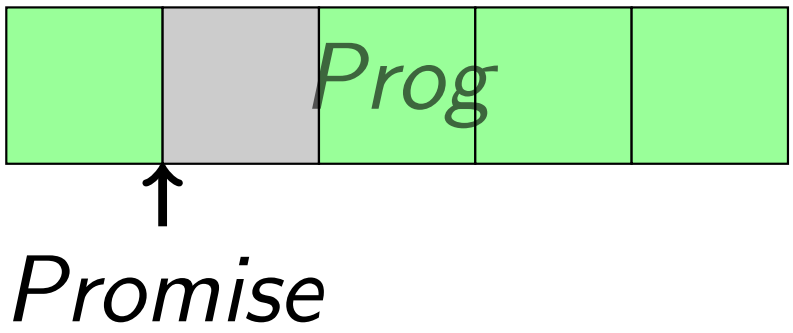

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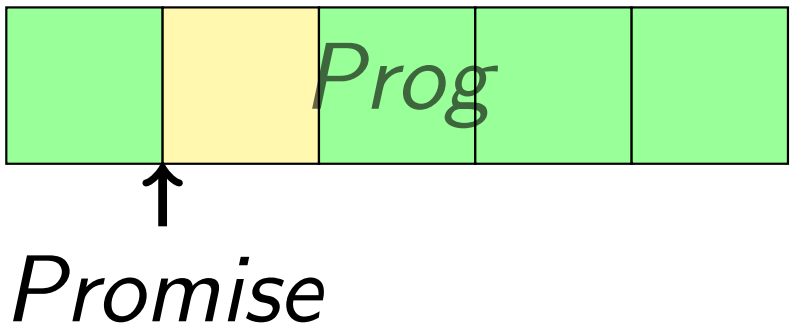

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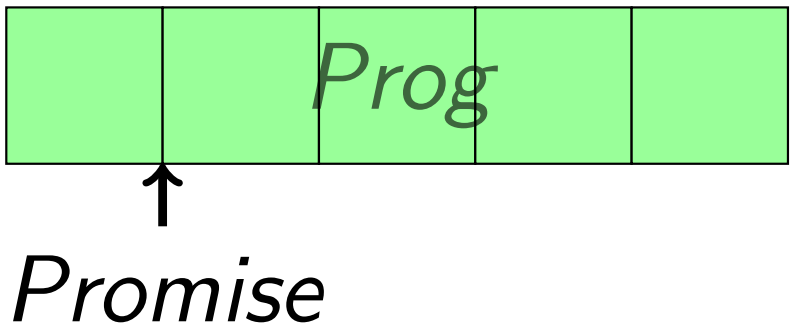

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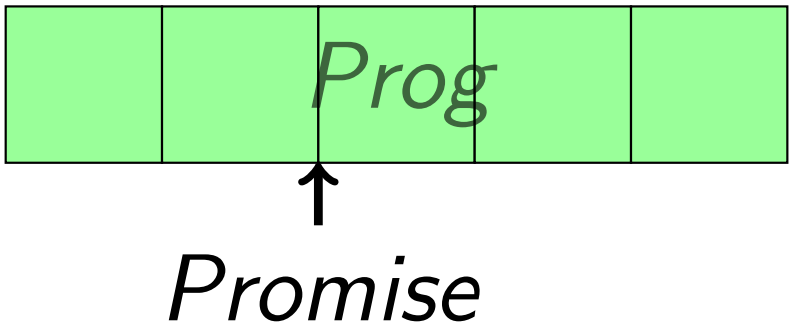

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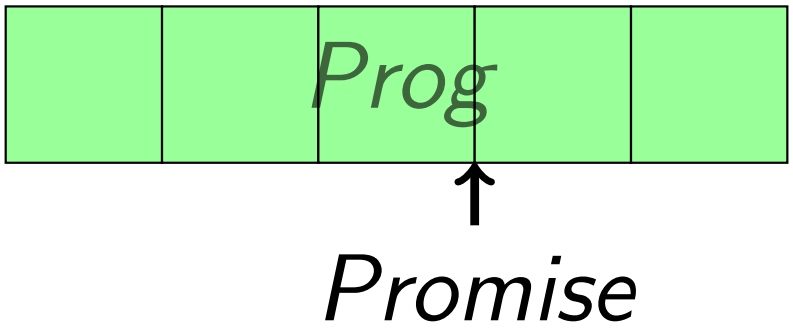

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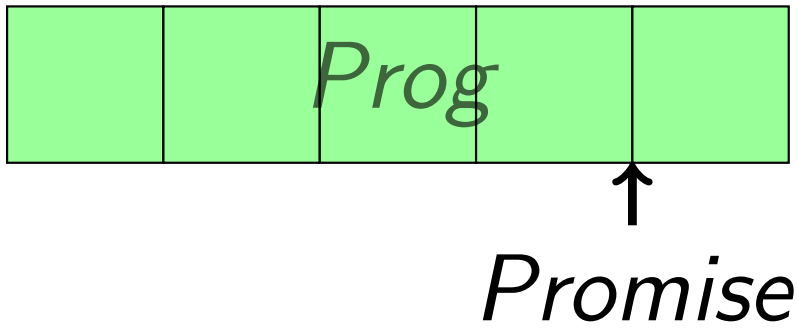

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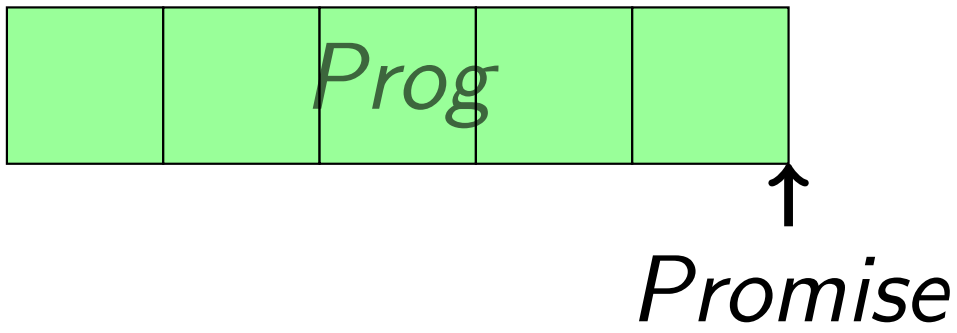

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“Запаздывающая” симуляция. Формально

Лемма 1:
$\forall (\mathbf{a}, \mathbf{p}) \in \mathcal{I}_{\text{pre}}, \exists \mathbf{p}', \mathbf{p} \xrightarrow[\text{Promise}]{} \mathbf{p}', (\mathbf{a}, \mathbf{p}') \in \mathcal{I}_{\text{pre}} \cup \mathcal{I}.$

Лемма 2:
$\forall (\mathbf{a}, \mathbf{p}) \in \mathcal{I}_{\text{pre}}, \exists n, \{\mathbf{p}_i\}_{i \in [0,n]}, \mathbf{p}_0 = \mathbf{p}, (\forall i < n, \mathbf{p}_i \xrightarrow[\text{Promise}]{} \mathbf{p}_{i+1}),$
$(\forall i < n, (\mathbf{a}, \mathbf{p}_i) \in \mathcal{I}_{\text{pre}}), (\mathbf{a}, \mathbf{p}_n) \in \mathcal{I}.$

Лемма 3:
$\forall (\mathbf{a}, \mathbf{p}) \in \mathcal{I},$
$(\forall \mathbf{a}', \mathbf{a} \xrightarrow[\text{ARM}+\tau]{\neg\ \textbf{Write commit}} \mathbf{a}' \Rightarrow (\mathbf{a}', \mathbf{p}) \in \mathcal{I}_{\text{pre}} \cup \mathcal{I}) \wedge$
$(\forall \mathbf{a}', \mathbf{a} \xrightarrow[\text{ARM}+\tau]{\textbf{Write commit}} \mathbf{a}' \Rightarrow \exists \mathbf{p}', \mathbf{p} \xrightarrow[\text{Promise}]{\textbf{Promise write}} \mathbf{p}', (\mathbf{a}', \mathbf{p}') \in \mathcal{I}_{\text{pre}} \cup \mathcal{I}).$

Лемма 4:
$\forall (\mathbf{a}, \mathbf{p}) \in \mathcal{I}, \mathbf{a}', \mathbf{a} \xrightarrow[\text{ARM}+\tau]{} \mathbf{a}' \Rightarrow$
$\exists \mathbf{p}', \mathbf{p} \xrightarrow[\text{Promise}]{}^{*} \mathbf{p}', (\mathbf{a}', \mathbf{p}') \in \mathcal{I}.$

Теорема:
$\forall \mathit{Prog}, \{\mathbf{a}_i\}_{i \in [0..n]},$
$\mathbf{a}^{\text{init}}(\mathit{compile}(\mathit{Prog})) = \mathbf{a}_0 \xrightarrow[\text{ARM}+\tau]{} \ldots \xrightarrow[\text{ARM}+\tau]{} \mathbf{a}_n, \text{Final}^{\text{ARM}+\tau}(\mathbf{a}_n),$
$\exists \{\mathbf{p}_i\}_{i \in [0..k]},$
$\mathbf{p}^{\text{init}}(\mathit{Prog}) = \mathbf{p}_0 \xrightarrow[\text{Promise}]{} \ldots \xrightarrow[\text{Promise}]{} \mathbf{p}_k, \text{Final}^{\text{Promise}}(\mathbf{p}_k),$
$\text{same-memory}(\mathbf{a}_n, \mathbf{p}_k).$

Promising Compilation to ARMv8

Anton Podkopaev[1], Ori Lahav[2], and Viktor Vafeiadis[2]

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Abstract

We prove the correctness of compilation of relaxed memory accesses and release-acquire fences from the "promising" semantics of Kang et al. [8] to the ARMv8 POP machine of Flur et al. [5]. The proof is highly non-trivial, because both the ARMv8 and the promising semantics provide some extremely weak consistency guarantees for normal memory accesses; however, they do so in rather different ways. Being the first formal proof about the ARMv8 POP model, in the process we also had to formalize the semantics of Flur et al. Our proof of compilation correctness to ARMv8 strengthens the results of the Kang et al., who only proved correctness of compilation to x86-TSO and Power, which are much simpler in comparison to ARMv8.

1998 ACM Subject Classification F.3.1 Specifying and Verifying and Reasoning about Programs

Keywords and phrases ARM, Compilation Correctness, Weak Memory Model

Digital Object Identifier 10.4230/LIPIcs...

1 Introduction

One of the major unresolved topics in the semantics of programming languages has to do with giving semantics to concurrent shared-memory programs. While it is well understood that such programs cannot follow the naive paradigm of *sequential consistency* (SC) [11], it is not completely clear what the right semantics of such concurrent programs should be.

At the level of machine code, the semantics varies a lot depending on the hardware architecture, which is only loosely specified by the vendor manuals. In the last decade, academic researchers have produced formal models for the mainstream hardware architectures (e.g., x86-TSO [17], Power [16, 1], ARMv8 [5]) by engaging in discussions with hardware architects and subjecting existing hardware implementations to extensive tests.

In this paper, we will focus on the ARMv8 model due to Flur et al. [5], which is the most recent and arguably the most advanced such hardware memory model. Operational in nature, it models many low-level hardware features that affect the execution of concurrent

Планы на будущее

- Поддержка остальных конструкций “обещающей” семантики

  (Read-Modify-Writes, Release/Acquire accesses, SC fences)

- Механизация доказательства в Coq

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Спасибо!

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In *TPHOLs*, volume 5674 of *LNCS*, pages 391–407. Springer.

The first step is a **formal semantics**

PL semantics should

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- allow high-level reasoning.

	Eff. Impl.	Comp. Opt.	H.-l. Reasoning
Lamport's SC	✗	✗	✓
C/C++11 MM	✓	✓	✗
Java MM	✓	✗	✓

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A promising semantics			
[Kang et al., 2017]	✓	✓	✓

The Promise machine [Kang et al., 2017] is **proved** to be **compilable** to x86 and Power.

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- x86 = SC + transformations,
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- x86 = SC + transformations,
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- the transformations are proved to be **sound** in the Promise machine;
- For every program, SC behaviors $\subset$ "StrongPower" behaviors $\subset$ behaviors of an axiomatic promise-free version of the Promise machine.

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The proof scheme isn't applicable to **ARM**

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Sketch of the proof:

The proof scheme isn't applicable to **ARM**
and here is why:

$\subset$ behaviors of an axiomatic promise-free version of the Promise machine.

$$[x] := 0; [y] := 0$$

$$\begin{array}{l|l|l} a := [x]; & b := [x]; & c := [y]; \\ [x] := 1 & [y] := b & [x] := c \end{array}$$

Allowed by ARMv8 [Flur et al., 2016]

$$[x] := 0; [y] := 0$$

$$\begin{array}{l|l|l} a := [x]; \ // \ 1 & b := [x]; & c := [y]; \\ [x] := 1 & [y] := b & [x] := c \end{array}$$

$$
\begin{array}{c}
[x] := 0; [y] := 0 \\
\begin{array}{l|l|l}
a := [x]; \ // \ 1 & b := [x]; & c := [y]; \\
[x] := 1 & [y] := b & [x] := c
\end{array}
\end{array}
$$

The behavior cannot be explained by transformations over a strong enough model.

Compilation scheme

Promise	ARM
$[x]_{\mathsf{rlx}} := a$	$[x] := a$
$a := [x]_{\mathsf{rlx}}$	$a := [x]$
fence acq	dmb LD
fence rel	dmb SY

Compilation scheme

Promise	ARM
fence acq	dmb LD
fence rel	dmb SY

As the compilation scheme is bijection, we use **one** syntax in examples.

Example 1

$$
\begin{array}{c}
[x] := 0; [y] := 0 \\
\hline
[x] := 1; \;\|\; a := [y]; \\
[y] := 1 \;\|\; b := [x]
\end{array}
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\begin{array}{c}
[x] := 0; [y] := 0 \\
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$$

Example 1

$$
\begin{array}{l}
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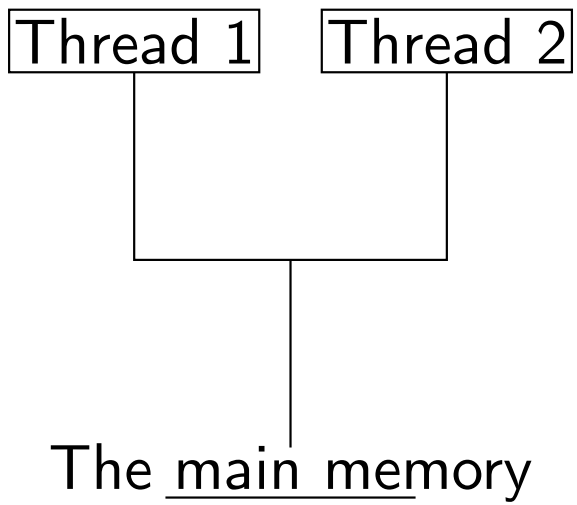

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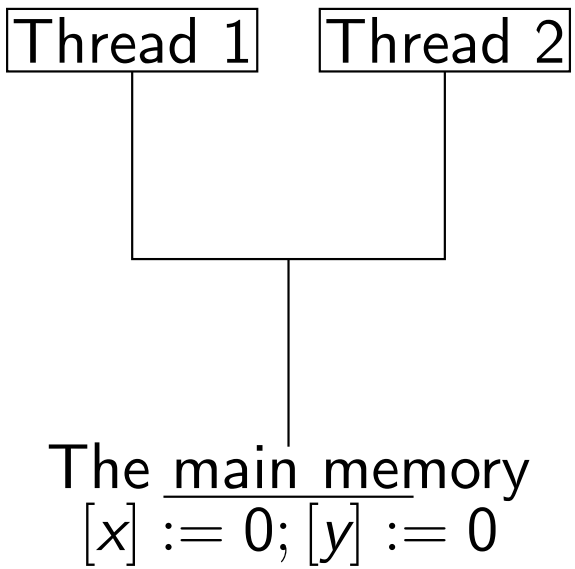

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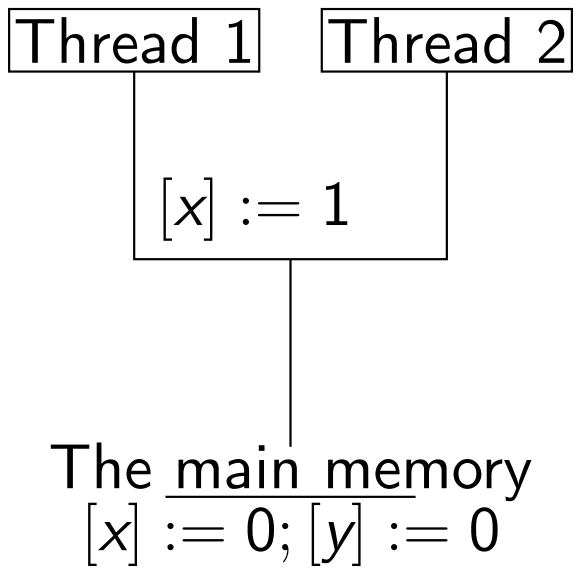

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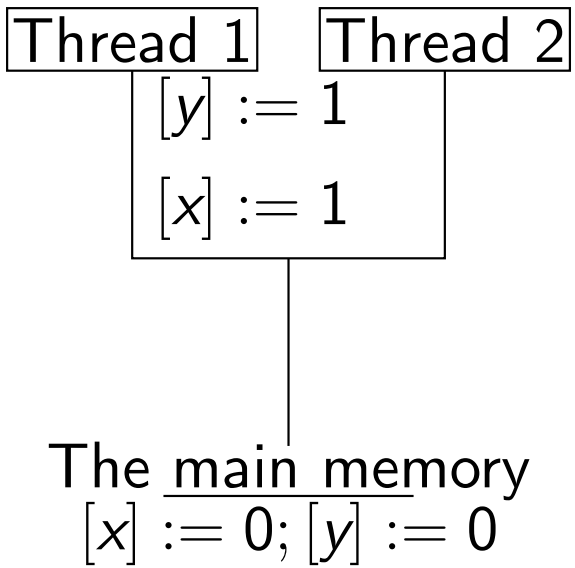

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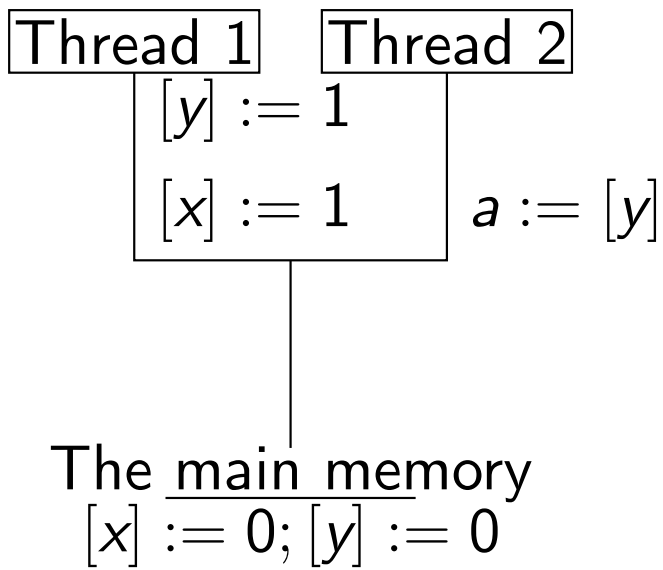

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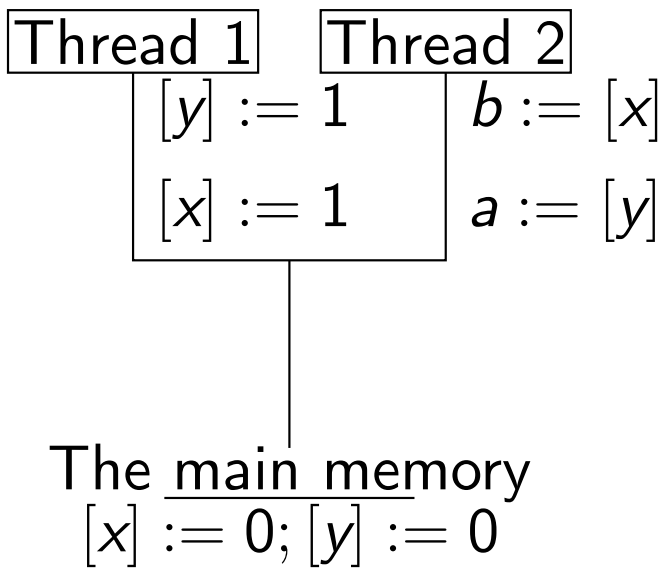

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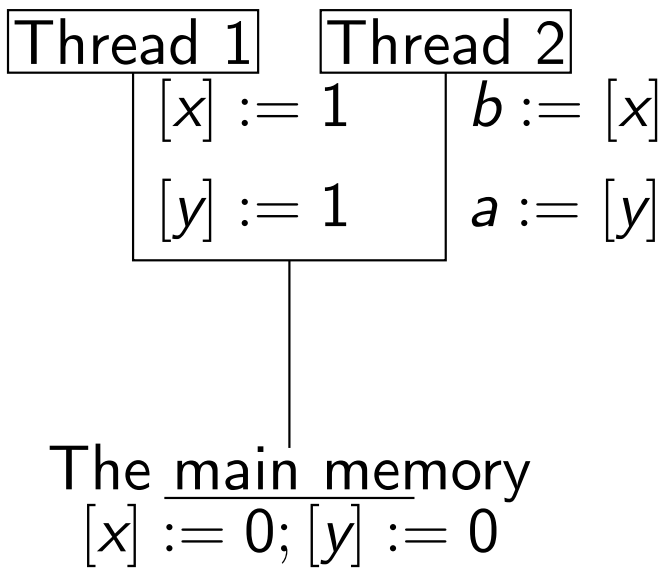

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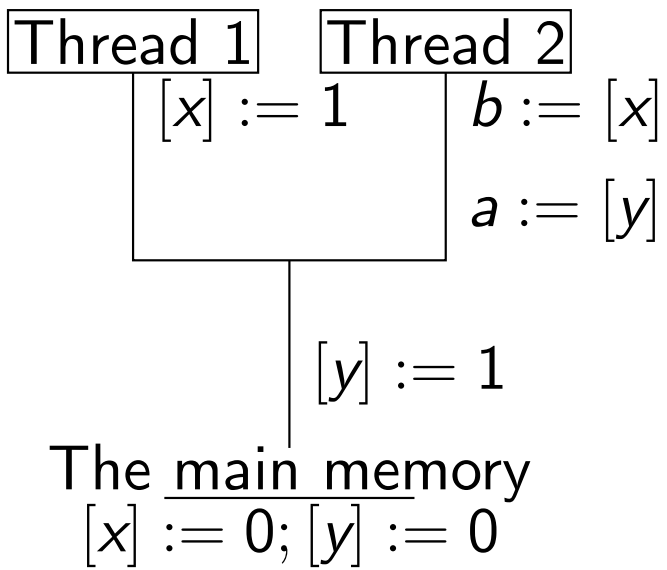
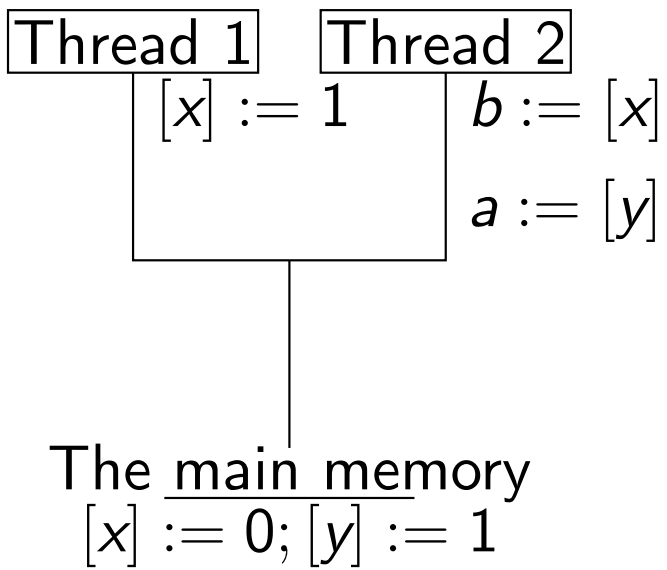
\end{array}
$$



Example 1

$$[x] := 0; [y] := 0$$

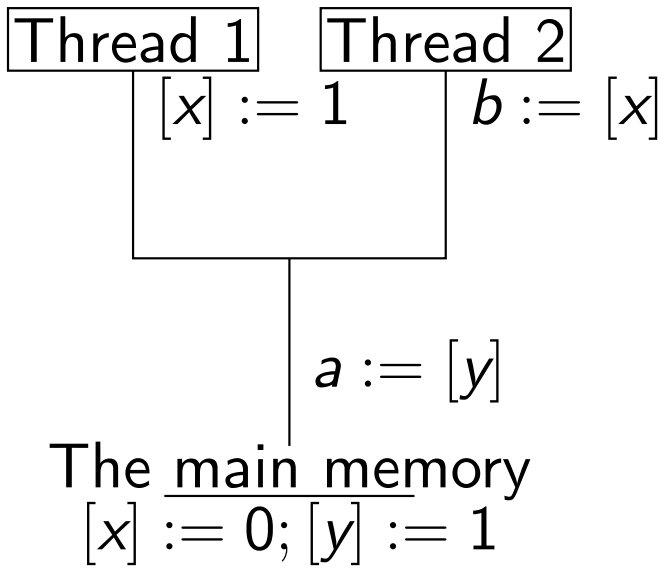
$$\begin{array}{l|l} [x] := 1; & a := [y]; \\ [y] := 1 & b := [x] \end{array}$$



Example 1

$$[x] := 0; [y] := 0$$

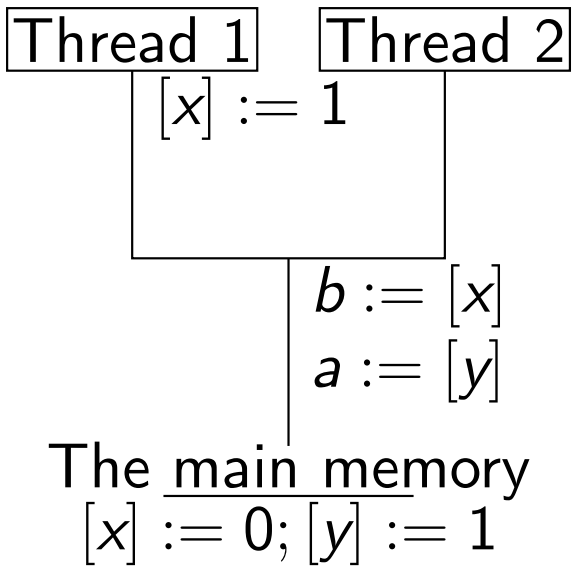
$$\begin{array}{l|l} [x] := 1; & a := [y]; \\ [y] := 1 & b := [x] \end{array}$$



Example 1

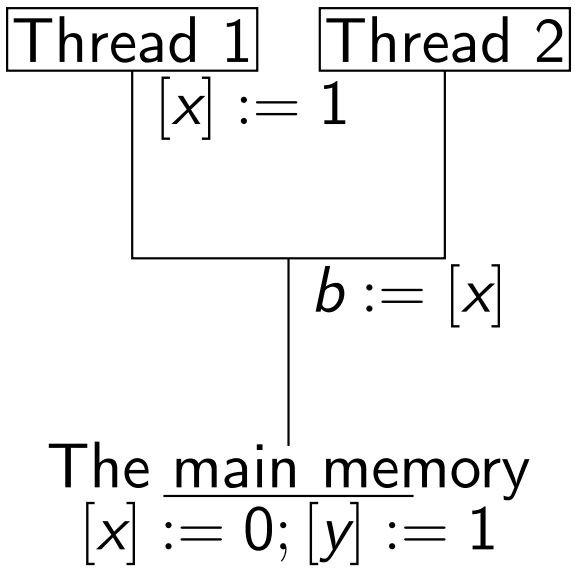
$$[x] := 0; [y] := 0$$

$$\begin{array}{l} [x] := 1; \\ [y] := 1 \end{array} \quad \| \quad \begin{array}{l} a := [y]; \\ b := [x] \end{array}$$



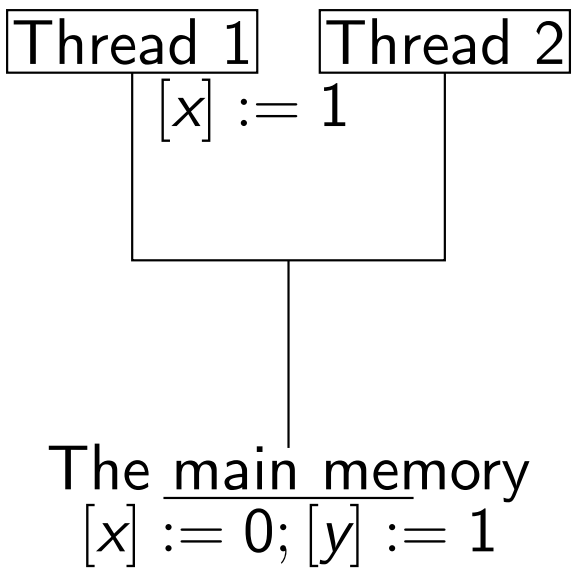
Example 1

$$
\begin{array}{l}
[x] := 0; [y] := 0 \\
\left.\begin{array}{l} [x] := 1; \\ [y] := 1 \end{array}\right. \;\Big\|\; \left.\begin{array}{l} a := [y]; \\ b := [x] \end{array}\right. \quad /\!/\ 1
\end{array}
$$



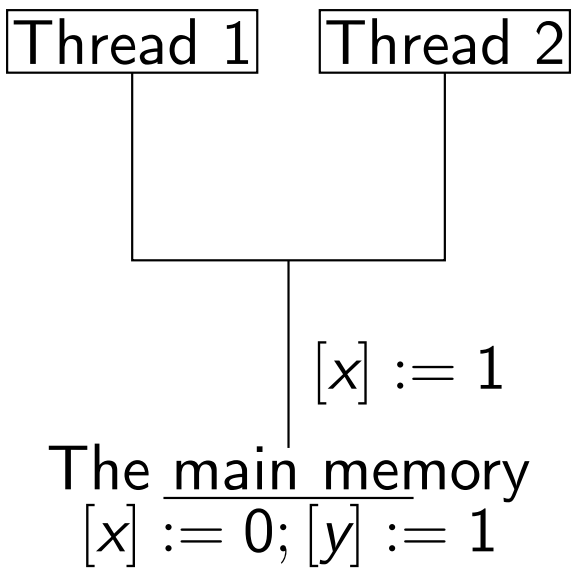
Example 1

$$
\begin{array}{l}
[x] := 0; [y] := 0 \\
\left.\begin{array}{l} [x] := 1; \\ [y] := 1 \end{array}\right. \;\Big\|\; \left.\begin{array}{l} a := [y]; \\ b := [x] \end{array}\right. \quad \begin{array}{l} /\!/\, 1 \\ /\!/\, 0 \end{array}
\end{array}
$$



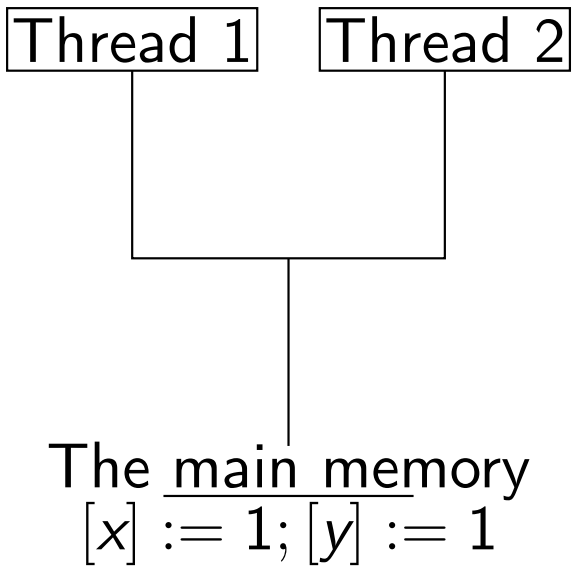
Example 1

$$
\begin{array}{l}
[x] := 0; [y] := 0 \\
\hline
[x] := 1; \;\|\; a := [y]; \quad // \; 1 \\
[y] := 1 \;\|\; b := [x] \quad // \; 0
\end{array}
$$



Example 1

$$
\begin{array}{l}
[x] := 0; [y] := 0 \\
\begin{array}{l|l|l}
[x] := 1; & a := [y]; & /\!/\ 1 \\
[y] := 1 & b := [x] & /\!/\ 0
\end{array}
\end{array}
$$



Example 2

$$
\begin{array}{c}
[x] := 0; [y] := 0 \\
\hline
[x] := 1; \;\|\; a := [y]; \\
\text{dmb SY}; \;\|\; \text{dmb LD}; \\
[y] := 1 \;\|\; b := [x]
\end{array}
$$

Example 2

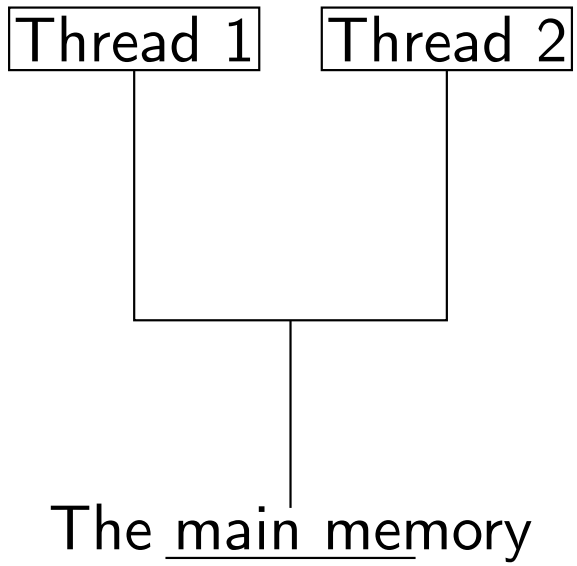
$$
\begin{array}{c}
[x] := 0; [y] := 0 \\
\hline
[x] := 1; \;\|\; a := [y]; \;\; /\!/\, 1 \\
\text{dmb SY}; \;\|\; \text{dmb LD}; \\
[y] := 1 \;\|\; b := [x]
\end{array}
$$

Example 2

$$
\begin{array}{c}
[x] := 0; [y] := 0 \\
\hline
[x] := 1; \;\|\; a := [y]; \;\; /\!/\, 1 \\
\text{dmb SY}; \;\|\; \text{dmb LD}; \\
[y] := 1 \;\|\; b := [x] \;\; /\!/\, 0
\end{array}
$$

Example 2

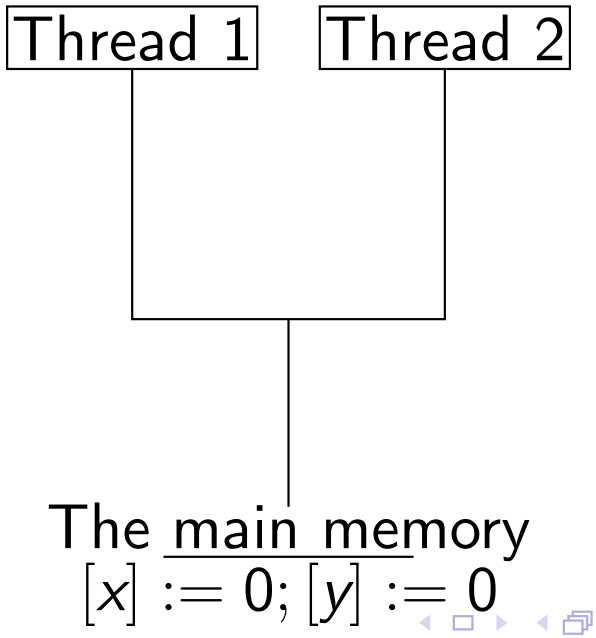
$$
\begin{array}{l}
[x] := 0; [y] := 0 \\
\hline
[x] := 1; \;\|\; a := [y]; \\
\text{dmb SY}; \;\|\; \text{dmb LD}; \\
[y] := 1 \;\|\; b := [x]
\end{array}
$$



Example 2

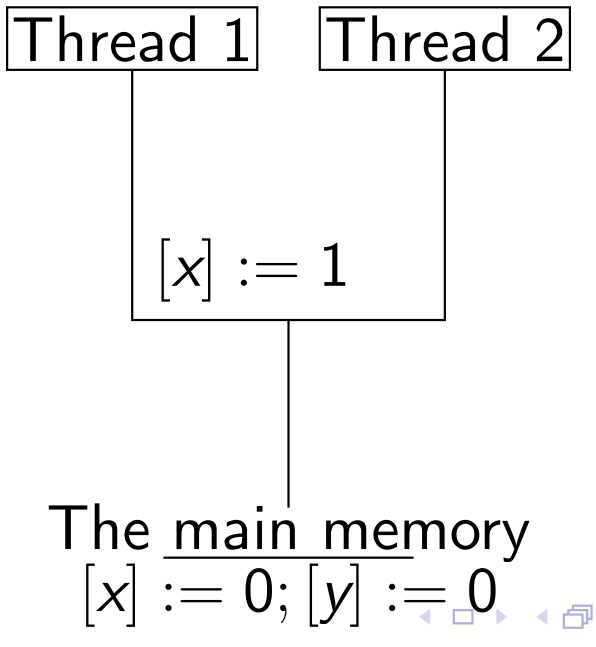
$[x] := 0; [y] := 0$

$[x] := 1;$	$a := [y];$
dmb SY;	dmb LD;
$[y] := 1$	$b := [x]$



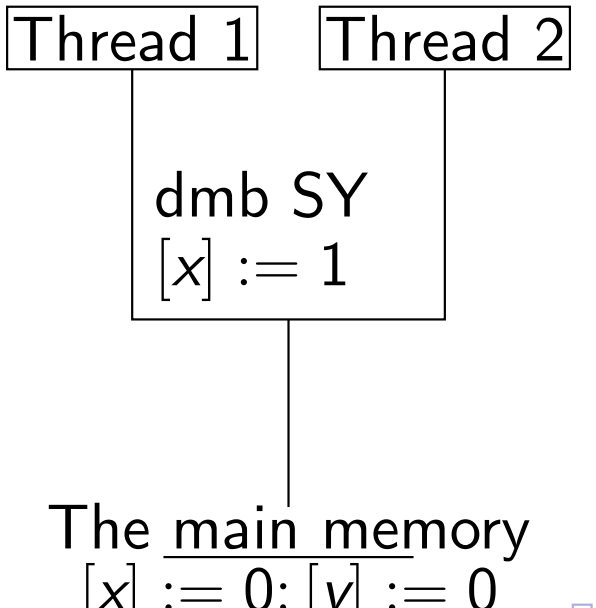
Example 2

$$
\begin{array}{l||l}
[x] := 0; [y] := 0 & \\
\hline
[x] := 1; & a := [y]; \\
\text{dmb SY}; & \text{dmb LD}; \\
[y] := 1 & b := [x]
\end{array}
$$



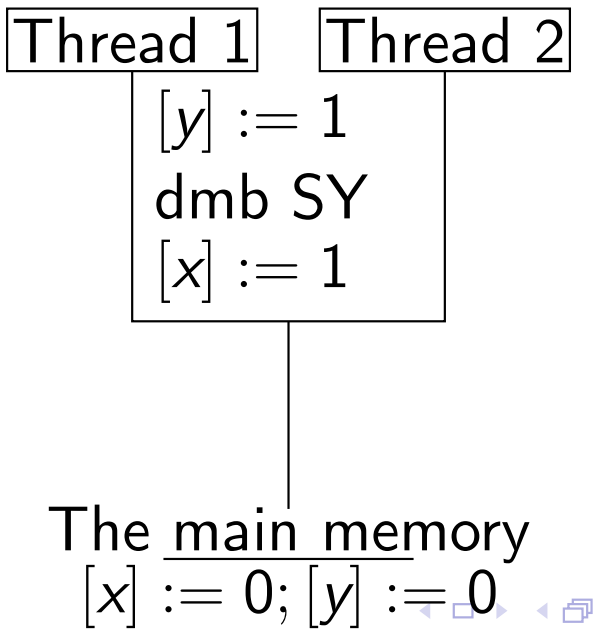
Example 2

$$
\begin{array}{l||l}
[x] := 0; [y] := 0 & \\
\hline
[x] := 1; & a := [y]; \\
\text{dmb SY}; & \text{dmb LD}; \\
[y] := 1 & b := [x]
\end{array}
$$



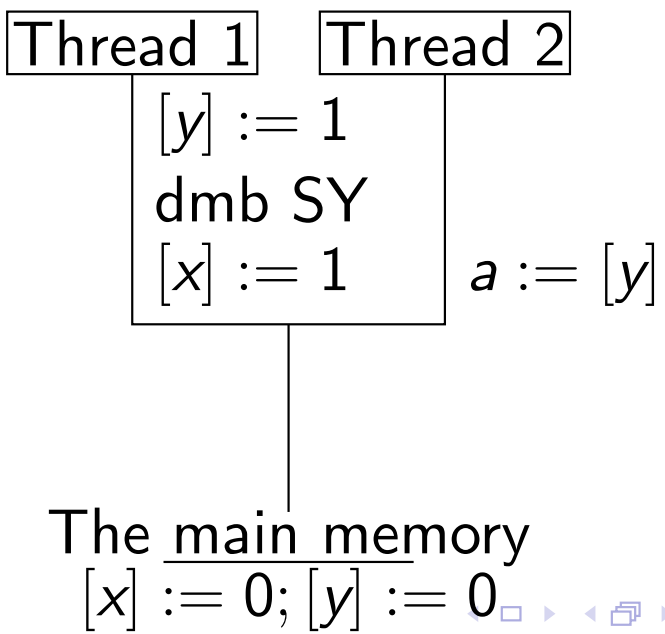
Example 2

$$
\begin{array}{l}
[x] := 0; [y] := 0 \\
\hline
[x] := 1; \quad \| \quad a := [y]; \\
\text{dmb SY}; \quad \| \quad \text{dmb LD}; \\
[y] := 1 \quad \| \quad b := [x]
\end{array}
$$

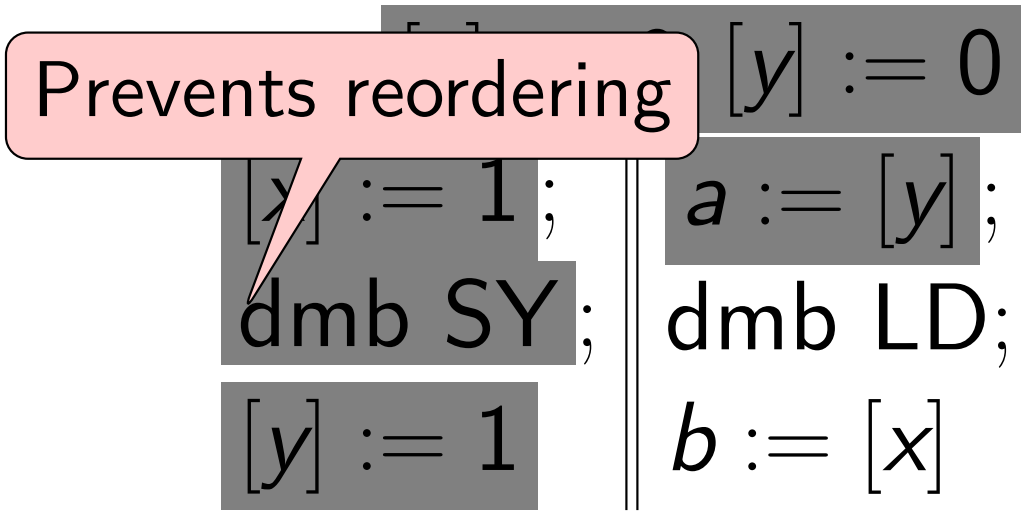


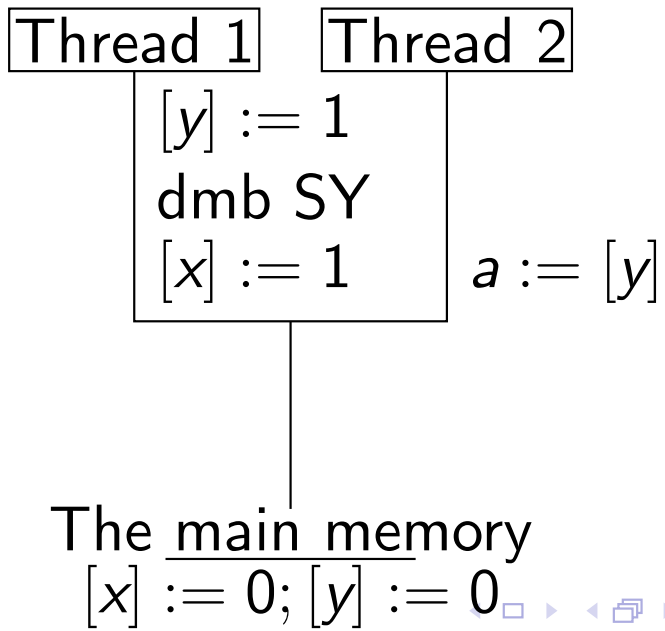
Example 2

$$
\begin{array}{l|l}
\multicolumn{2}{c}{[x] := 0; [y] := 0} \\
[x] := 1; & a := [y]; \\
\text{dmb SY}; & \text{dmb LD}; \\
[y] := 1 & b := [x]
\end{array}
$$

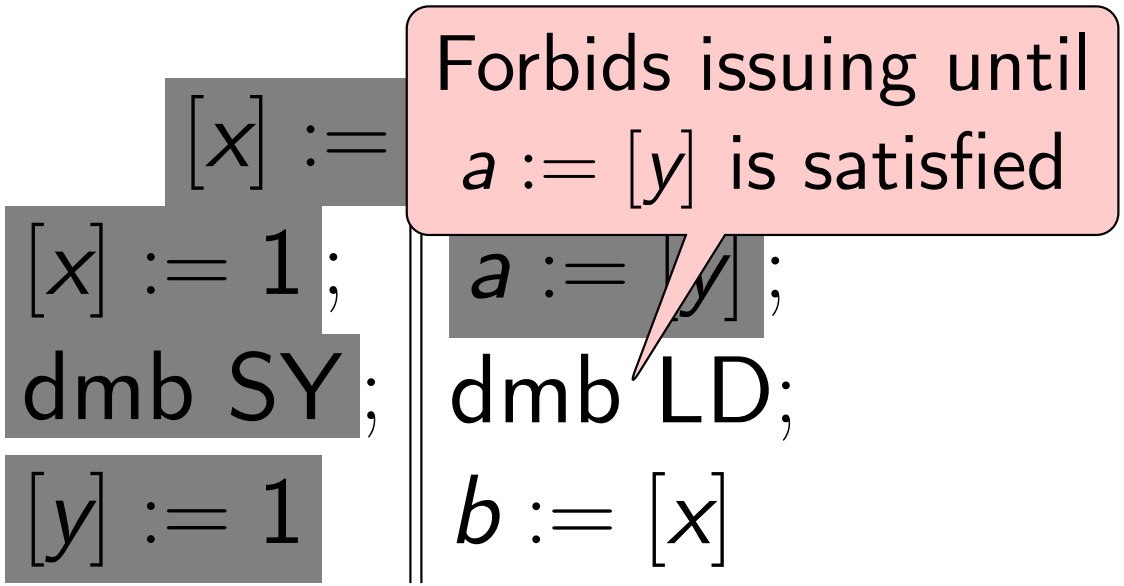


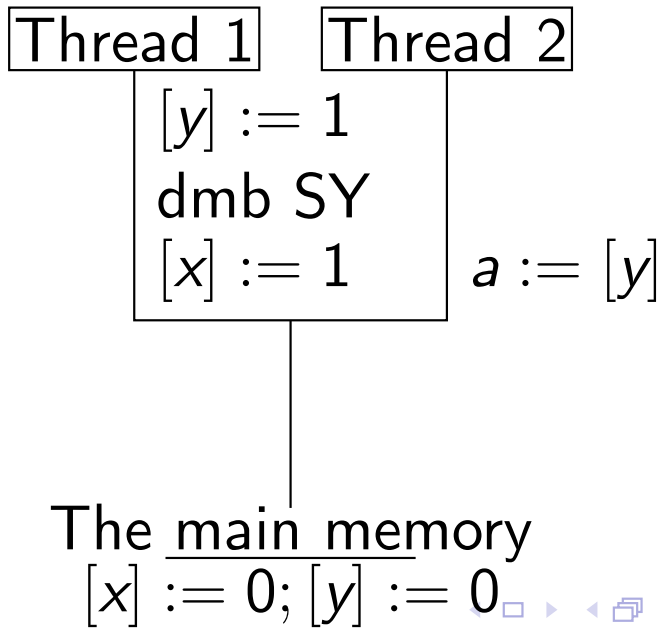
Example 2


Prevents reordering
[y] := 0
[x] := 1;
a := [y];
dmb SY;
dmb LD;
[y] := 1
b := [x]


Thread 1
Thread 2
[y] := 1
dmb SY
[x] := 1
a := [y]
The main memory
[x] := 0; [y] := 0

Example 2


Forbids issuing until
$a := [y]$ is satisfied
$[x] :=$
$[x] := 1$;
dmb SY;
$[y] := 1$
$a :=$ $[y]$;
dmb LD;
$b := [x]$


Thread 1
Thread 2
$[y] := 1$
dmb SY
$[x] := 1$
$a := [y]$
The main memory
$[x] := 0; [y] := 0$

Example 3

$$
\begin{array}{lll}
 & [x] := 0; [y] := 0 & \\
a := [x]; & \| \; b := [x]; & \| \; c := [y]; \\
[x] := 1 & \; [y] := b & \; [x] := c
\end{array}
$$

Example 3

$$
\begin{array}{lll}
 & [x] := 0; [y] := 0 & \\
a := [x]; \ // \ 1 \ \| & b := [x]; & \| \ c := [y]; \\
[x] := 1 & [y] := b & \| \ [x] := c
\end{array}
$$

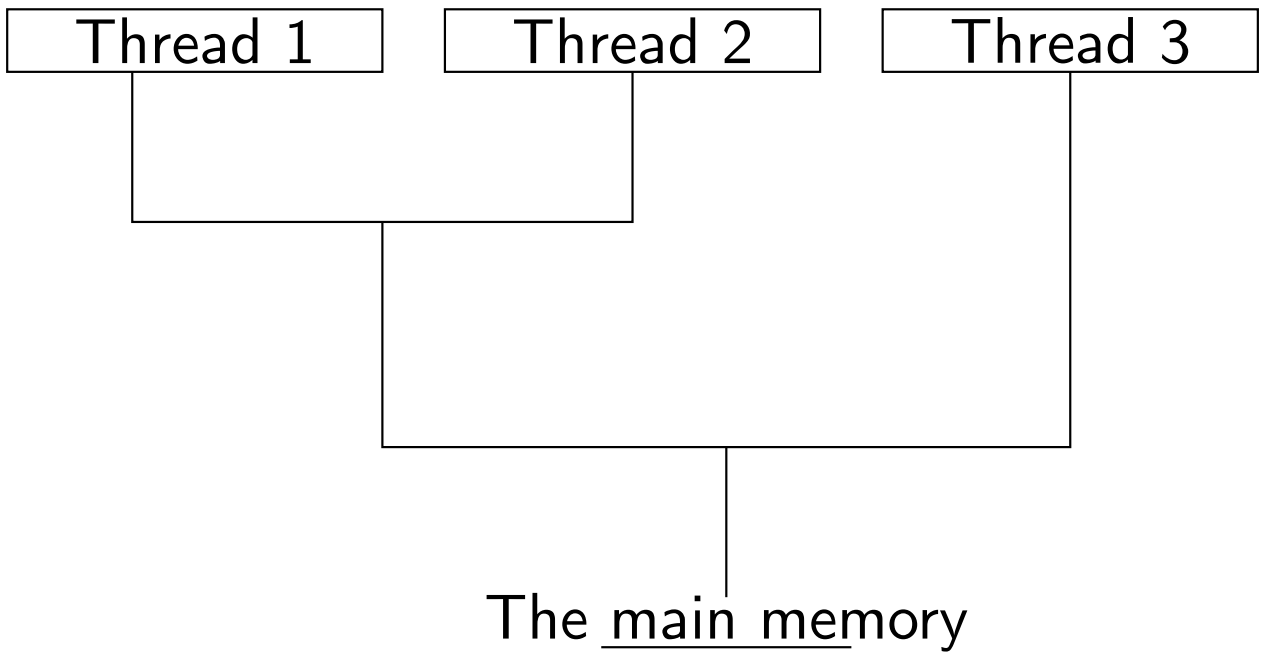
Example 3

$$
\begin{array}{lll}
 & [x] := 0; [y] := 0 & \\
a := [x]; & \| \; b := [x]; & \| \; c := [y]; \\
[x] := 1 & \; [y] := b & \; [x] := c
\end{array}
$$

Example 3

$$[x] := 0; [y] := 0$$

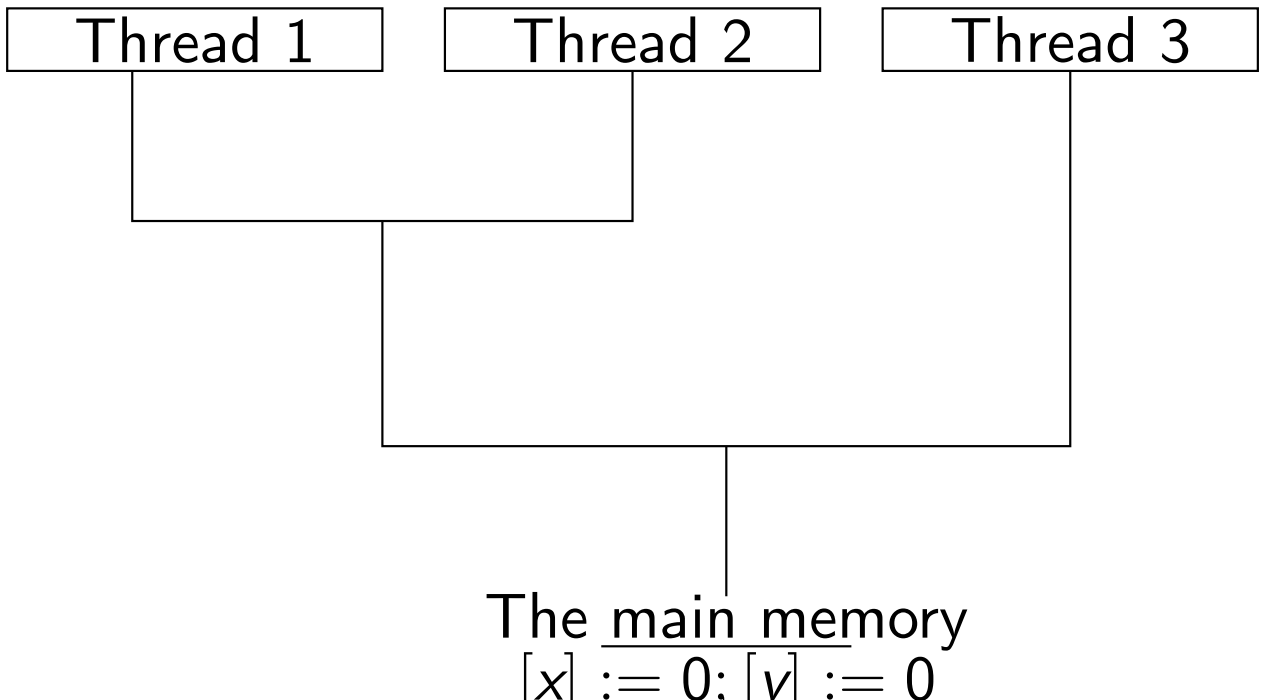
$$a := [x]; \quad [x] := 1 \quad \Big\| \quad b := [x]; \quad [y] := b \quad \Big\| \quad c := [y]; \quad [x] := c$$



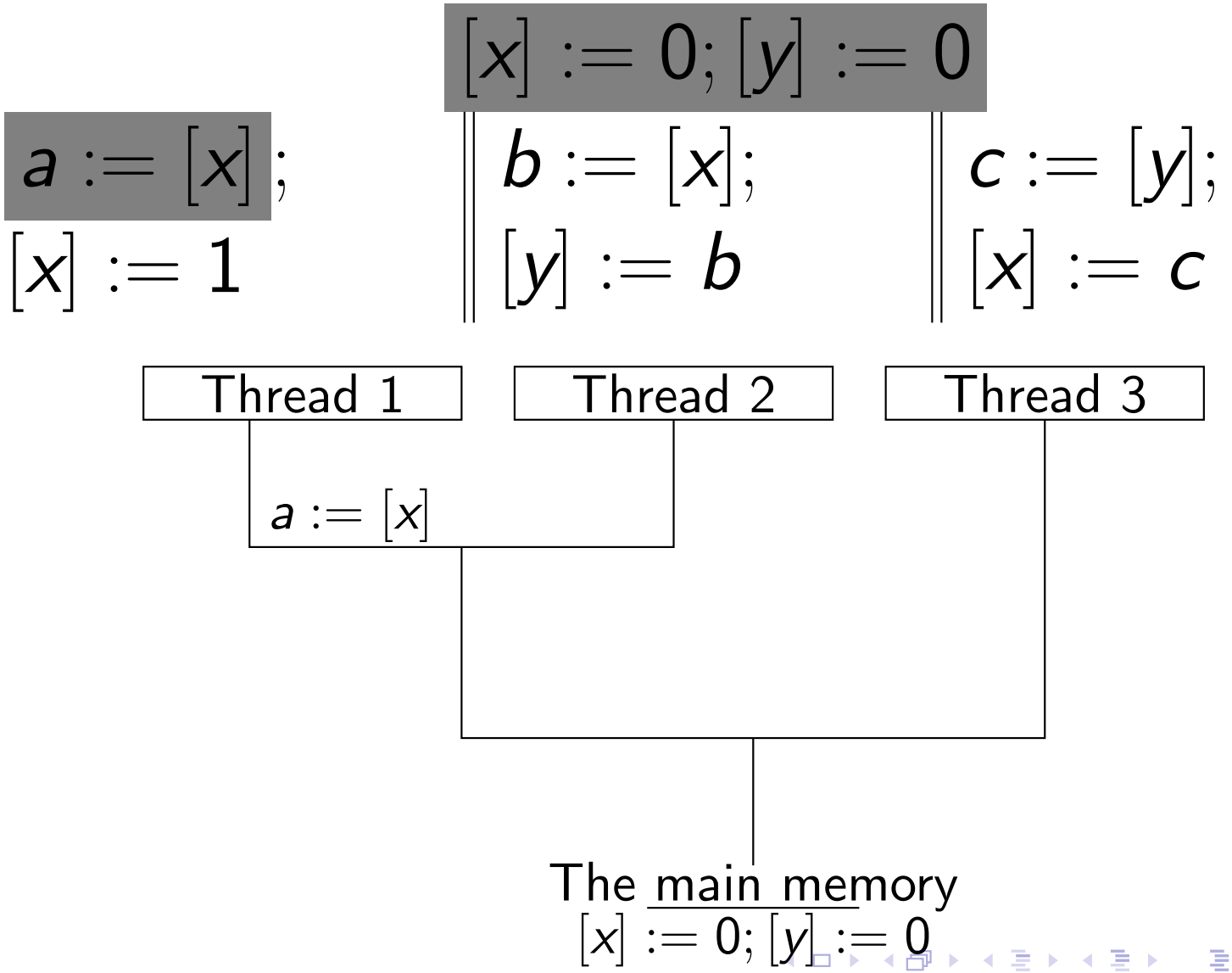
Example 3

$[x] := 0; [y] := 0$

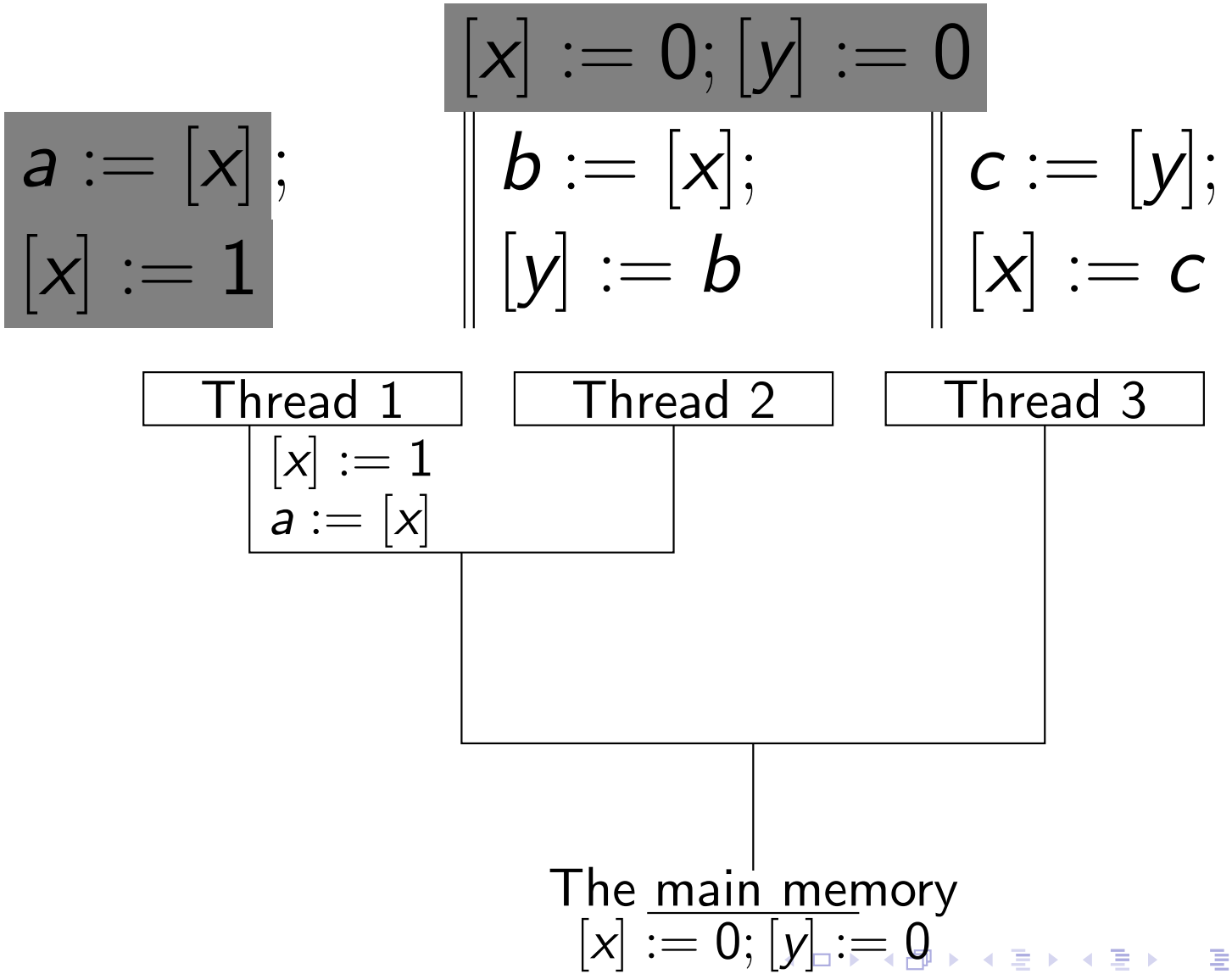
$a := [x];$ $[x] := 1$ || $b := [x];$ $[y] := b$ || $c := [y];$ $[x] := c$



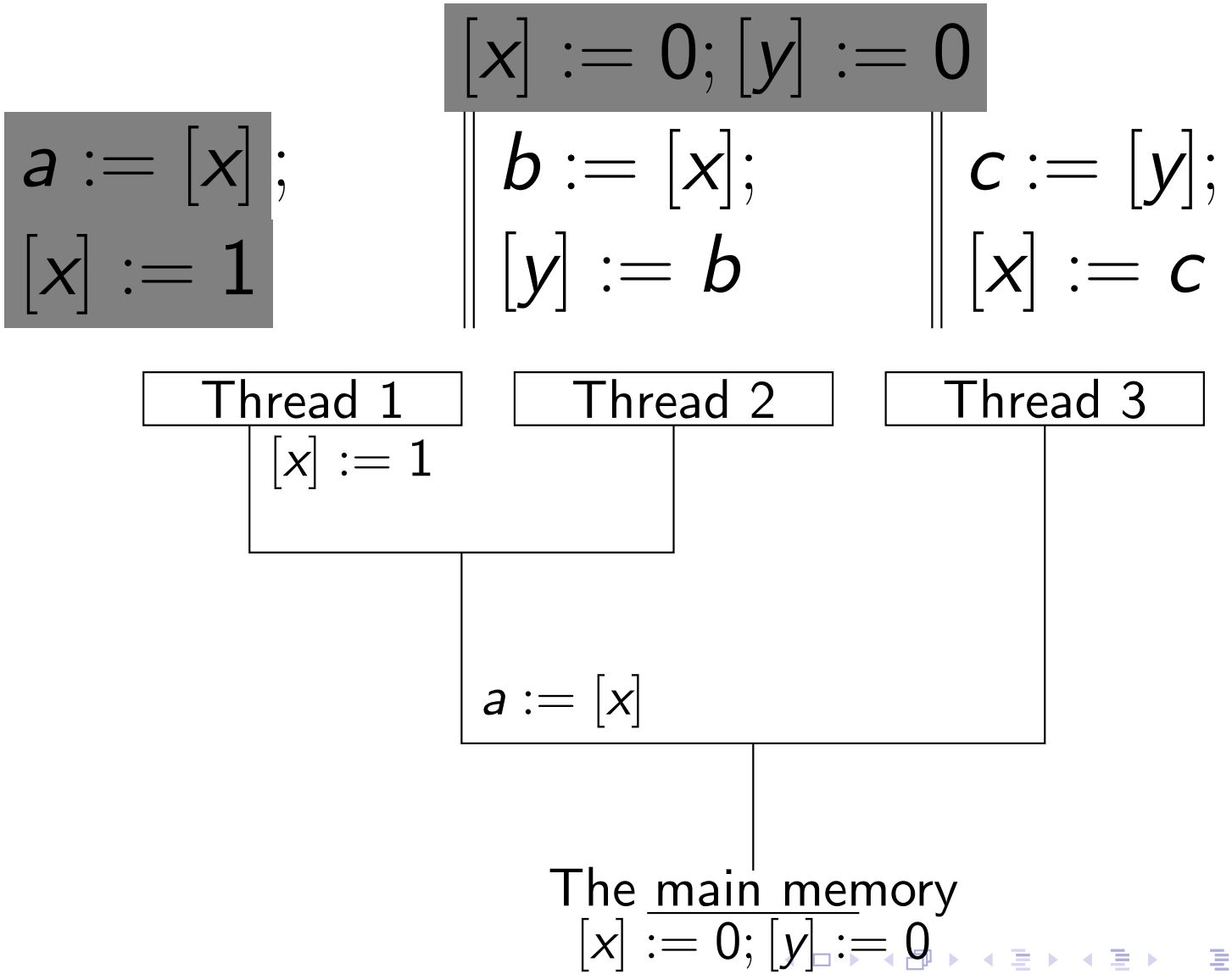
Example 3


[x] := 0; [y] := 0
a := [x];
[x] := 1
b := [x];
[y] := b
c := [y];
[x] := c
Thread 1
Thread 2
Thread 3
a := [x]
The main memory
[x] := 0; [y] := 0

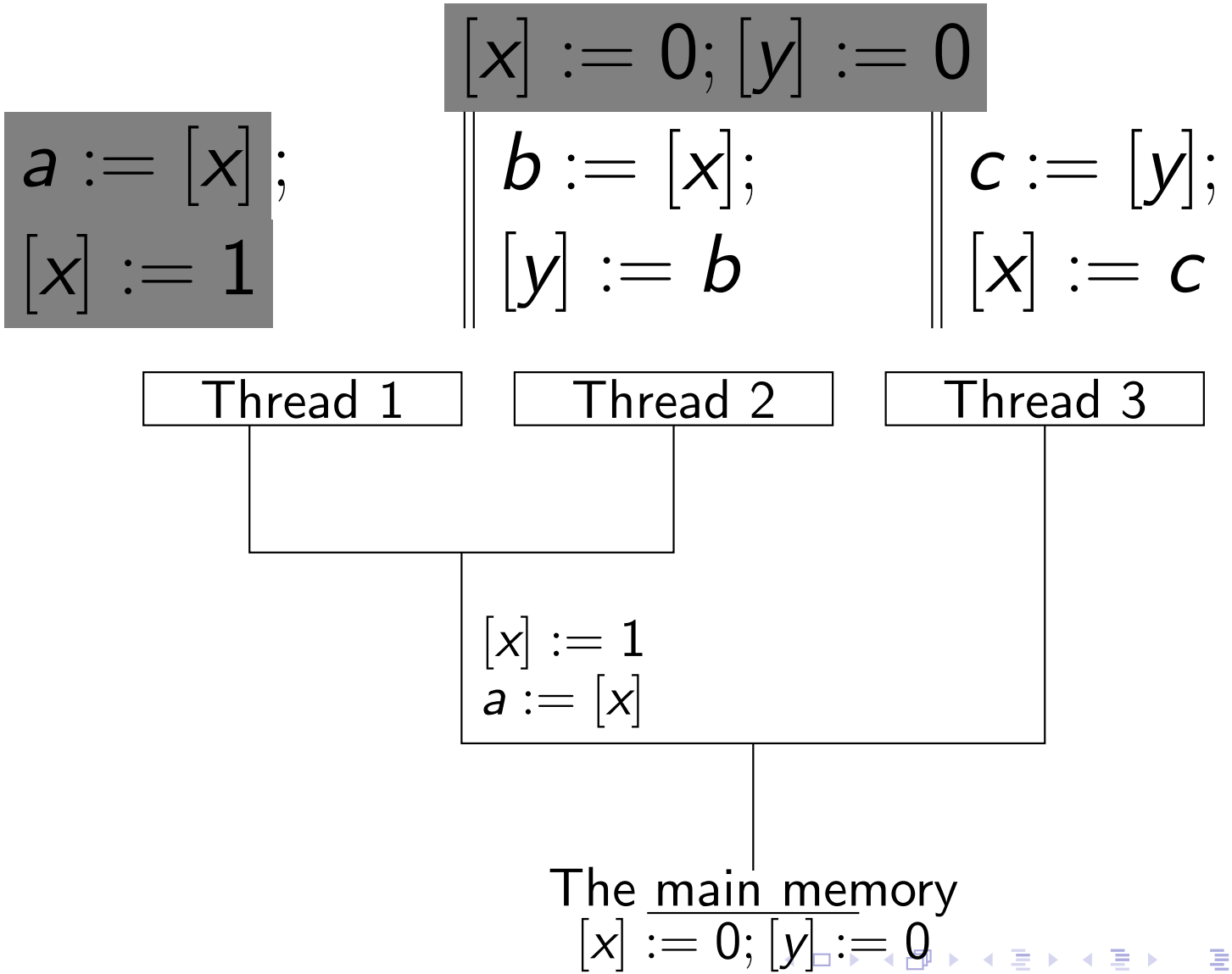
Example 3


[x] := 0; [y] := 0
a := [x];
[x] := 1
b := [x];
[y] := b
c := [y];
[x] := c
Thread 1
Thread 2
Thread 3
[x] := 1
a := [x]
The main memory
[x] := 0; [y] := 0

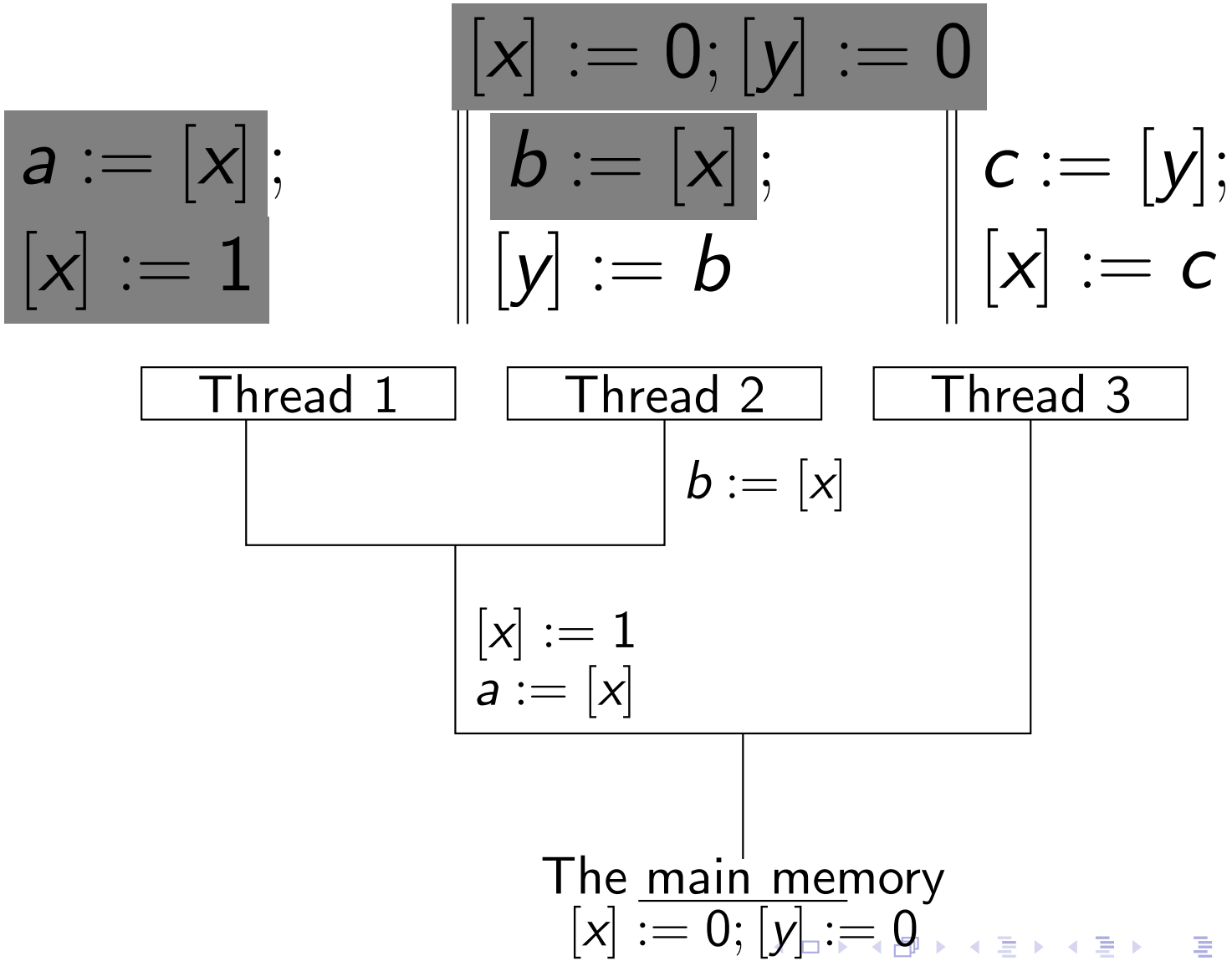
Example 3


[x] := 0; [y] := 0
a := [x];
[x] := 1
b := [x];
[y] := b
c := [y];
[x] := c
Thread 1
Thread 2
Thread 3
[x] := 1
a := [x]
The main memory
[x] := 0; [y] := 0

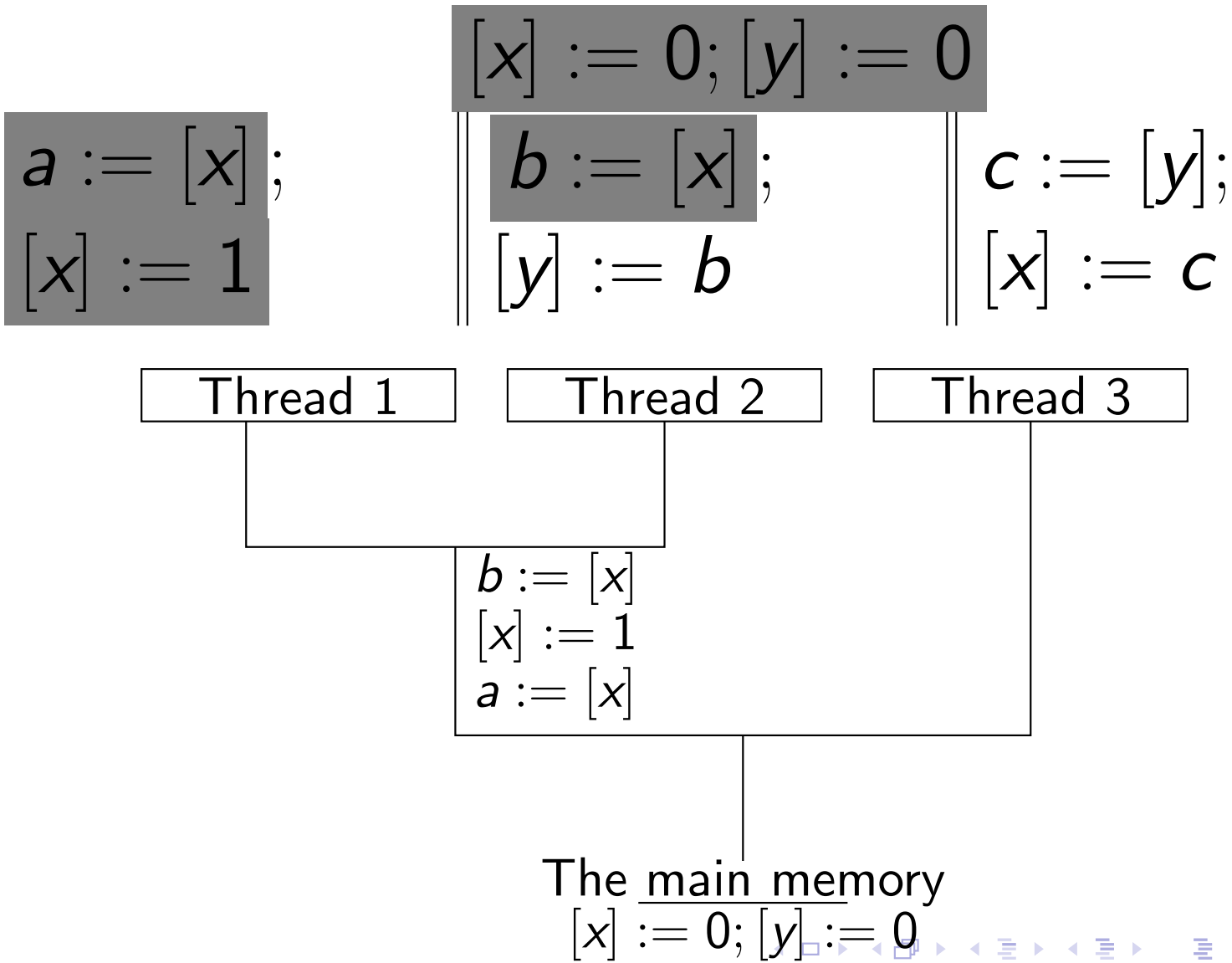
Example 3


[x] := 0; [y] := 0
a := [x]; [x] := 1
b := [x]; [y] := b
c := [y]; [x] := c
Thread 1
Thread 2
Thread 3
[x] := 1
a := [x]
The main memory
[x] := 0; [y] := 0

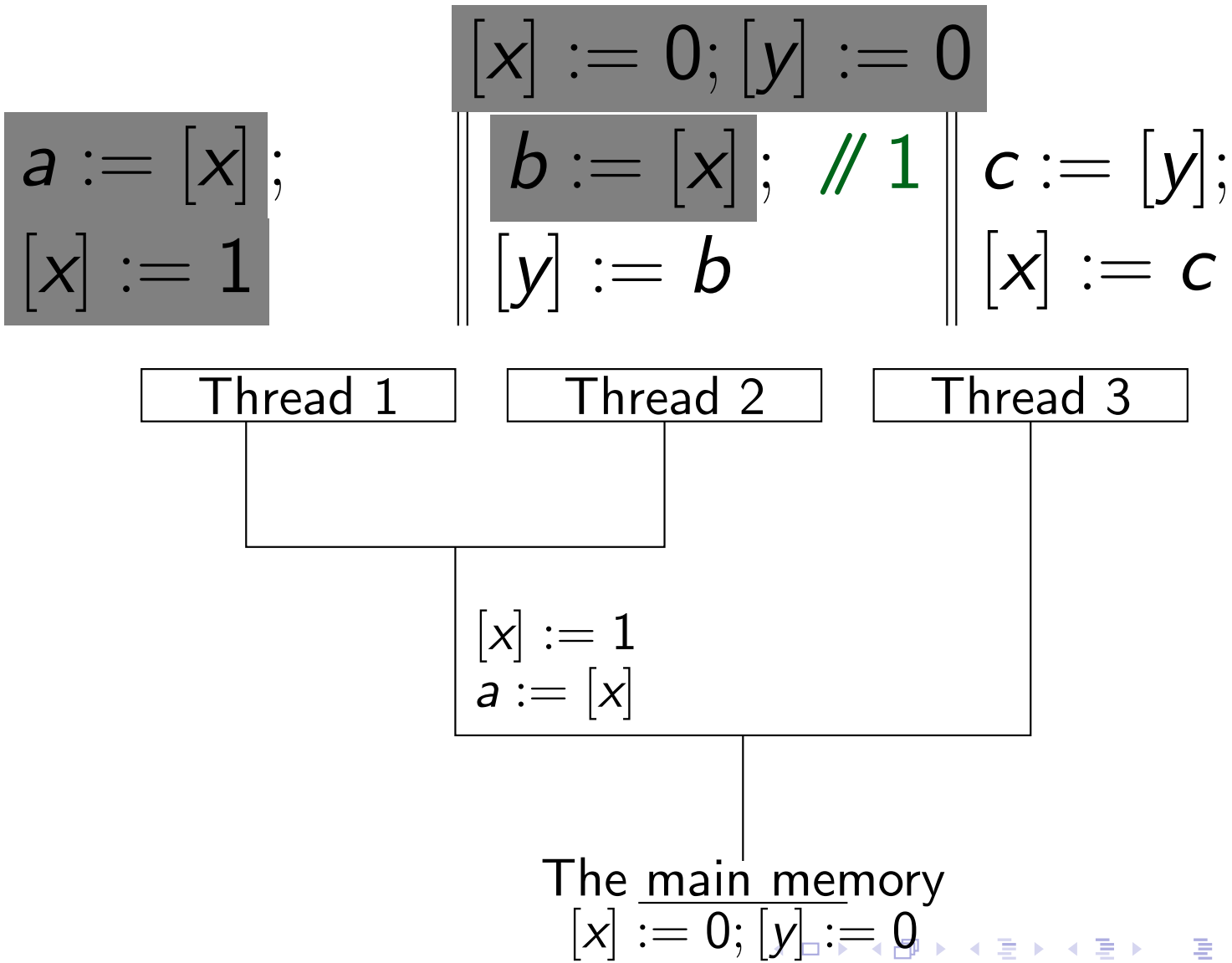
Example 3


[x] := 0; [y] := 0
a := [x]; [x] := 1
b := [x]; [y] := b
c := [y]; [x] := c
Thread 1
Thread 2
Thread 3
b := [x]
[x] := 1
a := [x]
The main memory
[x] := 0; [y] := 0

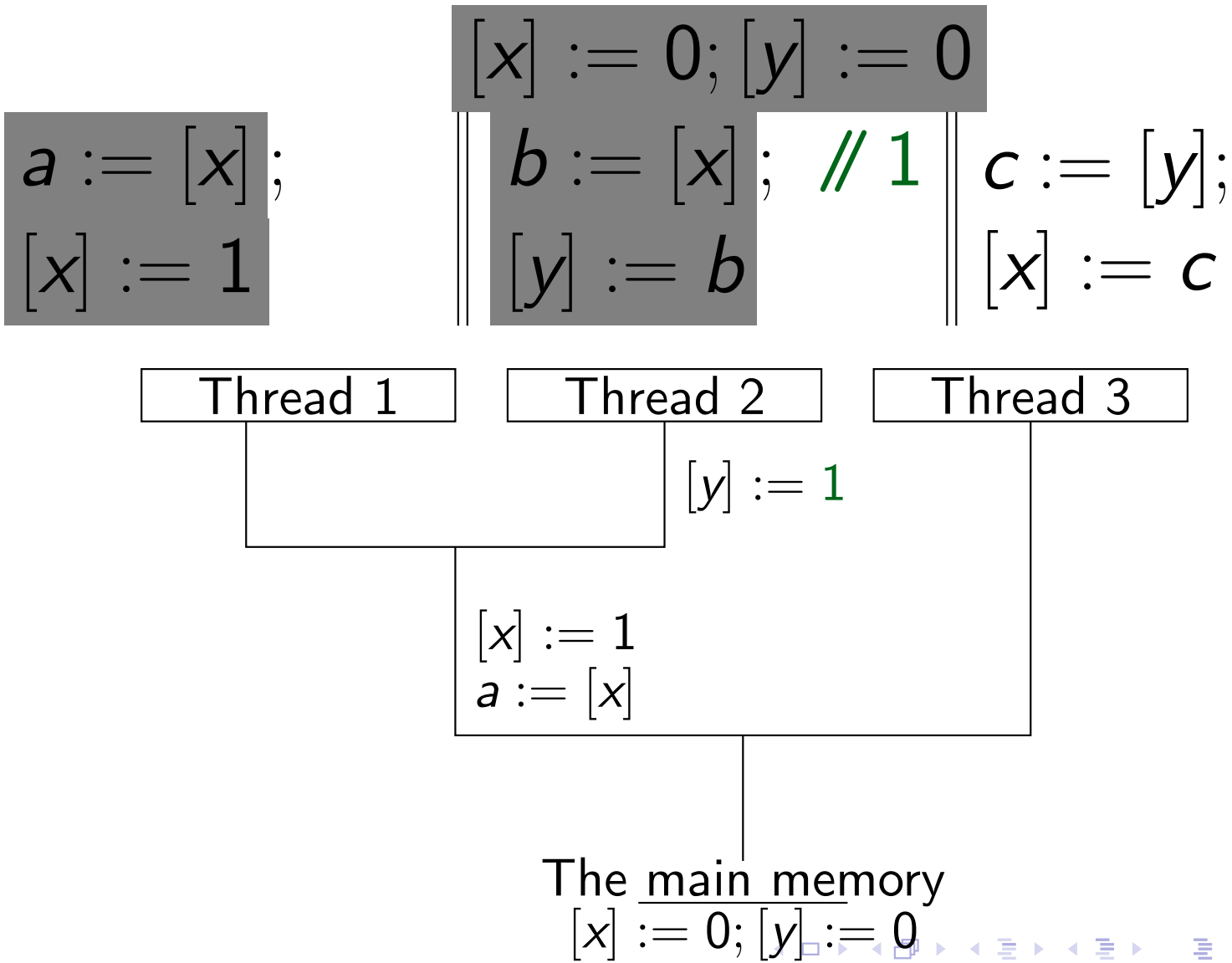
Example 3


[x] := 0; [y] := 0
a := [x];
[x] := 1
b := [x];
[y] := b
c := [y];
[x] := c
Thread 1
Thread 2
Thread 3
b := [x]
[x] := 1
a := [x]
The main memory
[x] := 0; [y] := 0

Example 3


[x] := 0; [y] := 0
a := [x];
[x] := 1
b := [x]; // 1
[y] := b
c := [y];
[x] := c
Thread 1
Thread 2
Thread 3
[x] := 1
a := [x]
The main memory
[x] := 0; [y] := 0

Example 3

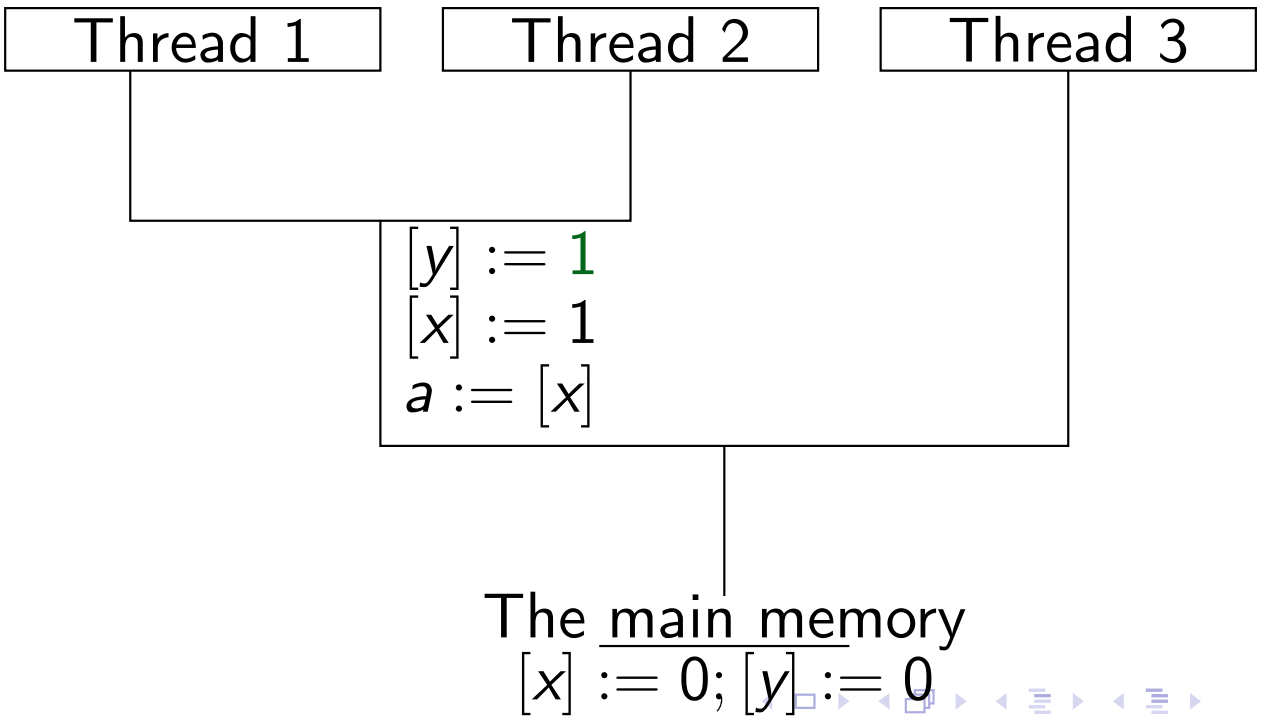

[x] := 0; [y] := 0
a := [x]; [x] := 1
b := [x]; // 1 [y] := b
c := [y]; [x] := c
Thread 1
Thread 2
Thread 3
[y] := 1
[x] := 1
a := [x]
The main memory
[x] := 0; [y] := 0

Example 3

$[x] := 0; [y] := 0$

$a := [x]; \quad \| \quad b := [x]; \; // \, 1 \quad \| \quad c := [y];$

$[x] := 1 \qquad\quad [y] := b \qquad\quad [x] := c$

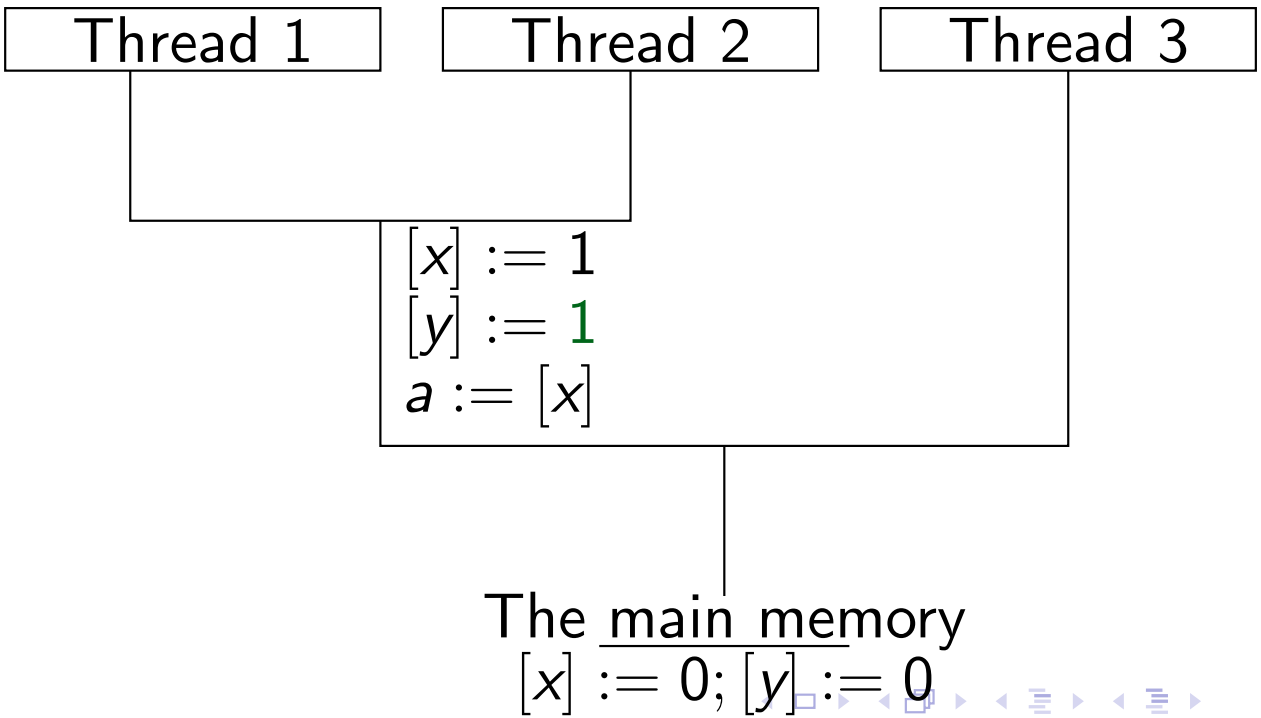


Example 3

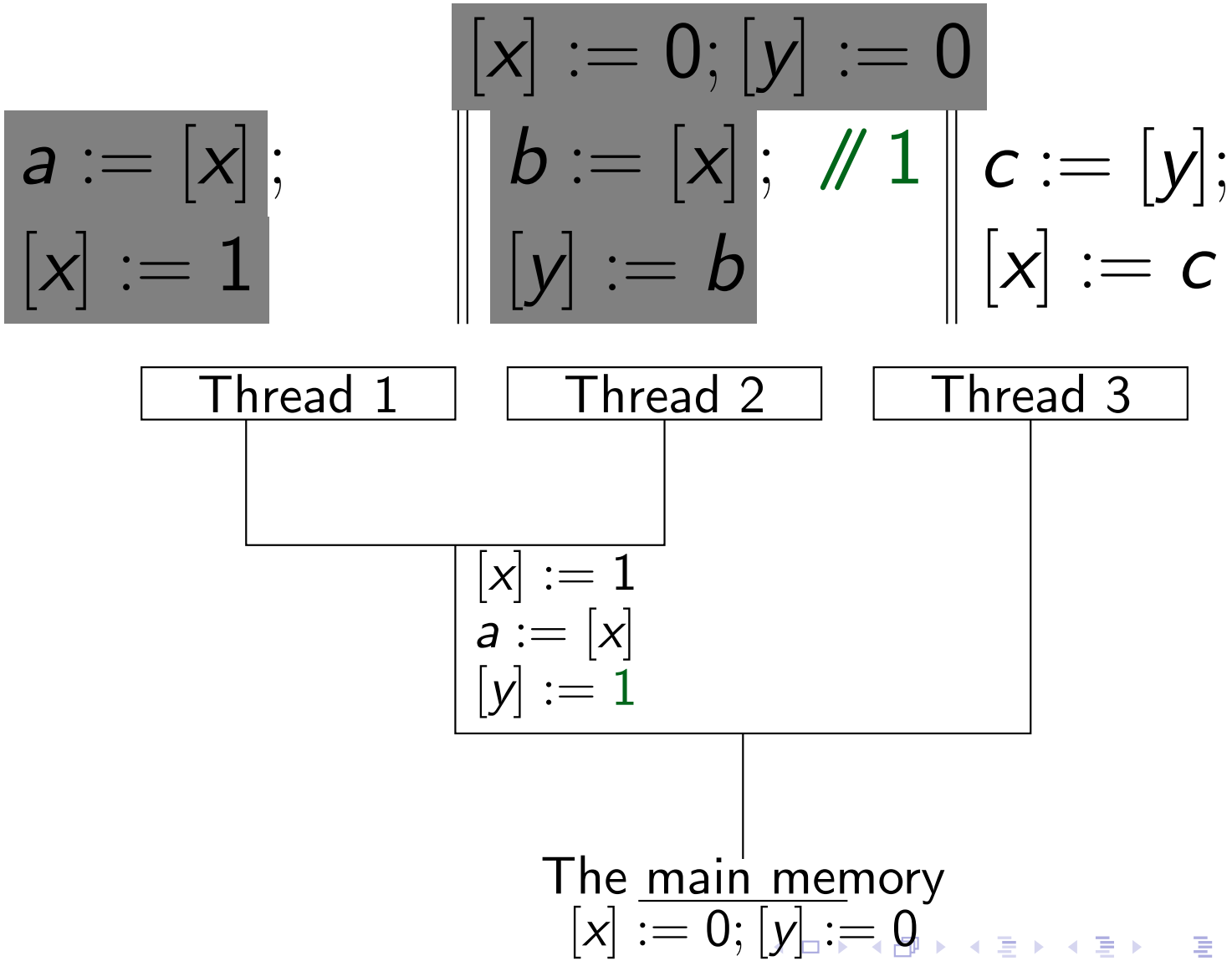
$[x] := 0; [y] := 0$

$a := [x]; \quad \| \quad b := [x]; \; // 1 \quad \| \quad c := [y];$

$[x] := 1 \qquad\quad [y] := b \qquad\quad [x] := c$



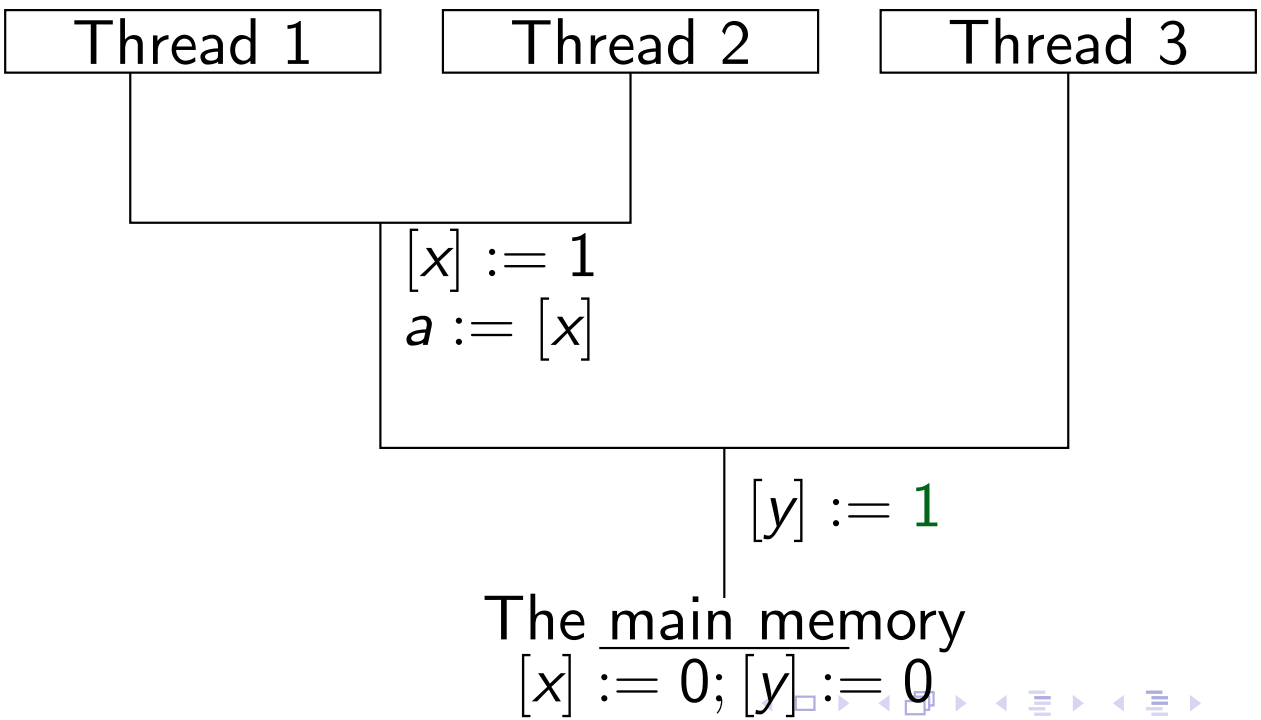
Example 3


[x] := 0; [y] := 0
a := [x]; [x] := 1
b := [x]; // 1
[y] := b
c := [y];
[x] := c
Thread 1
Thread 2
Thread 3
[x] := 1
a := [x]
[y] := 1
The main memory
[x] := 0; [y] := 0

Example 3

$[x] := 0; [y] := 0$

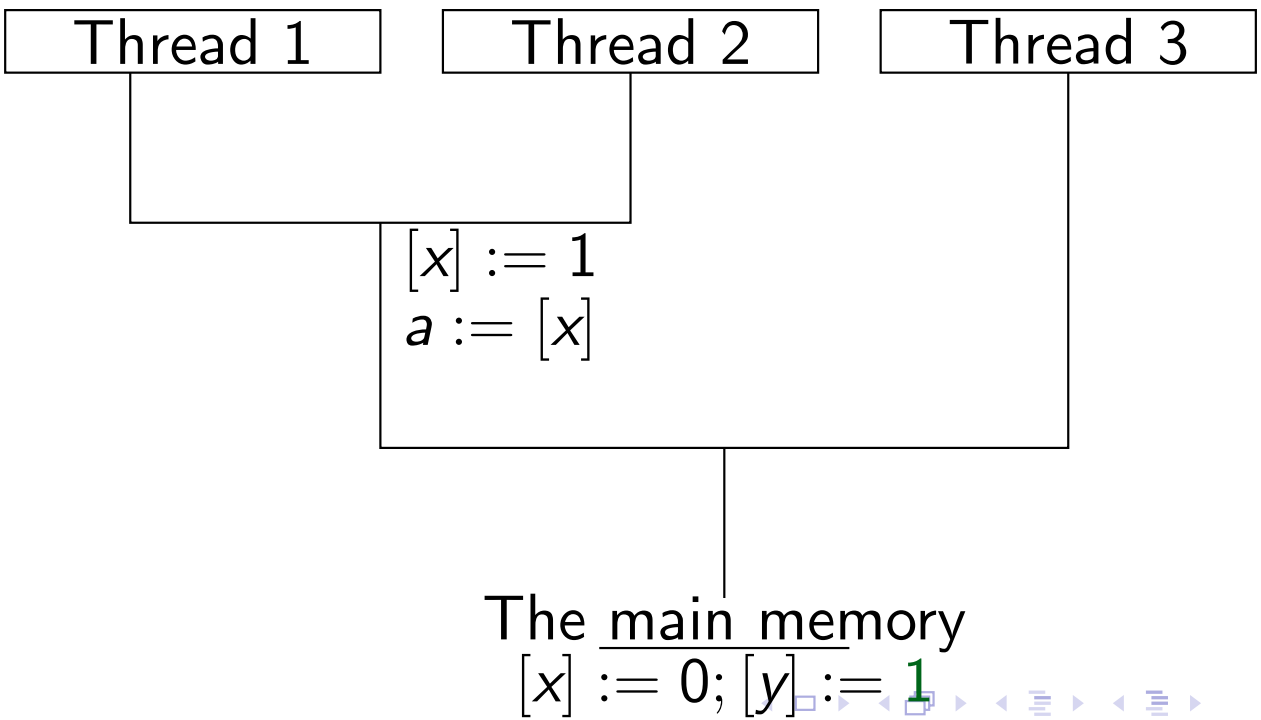
$a := [x]; \quad [x] := 1 \quad \| \quad b := [x]; \quad [y] := b \quad // 1 \quad \| \quad c := [y]; \quad [x] := c$



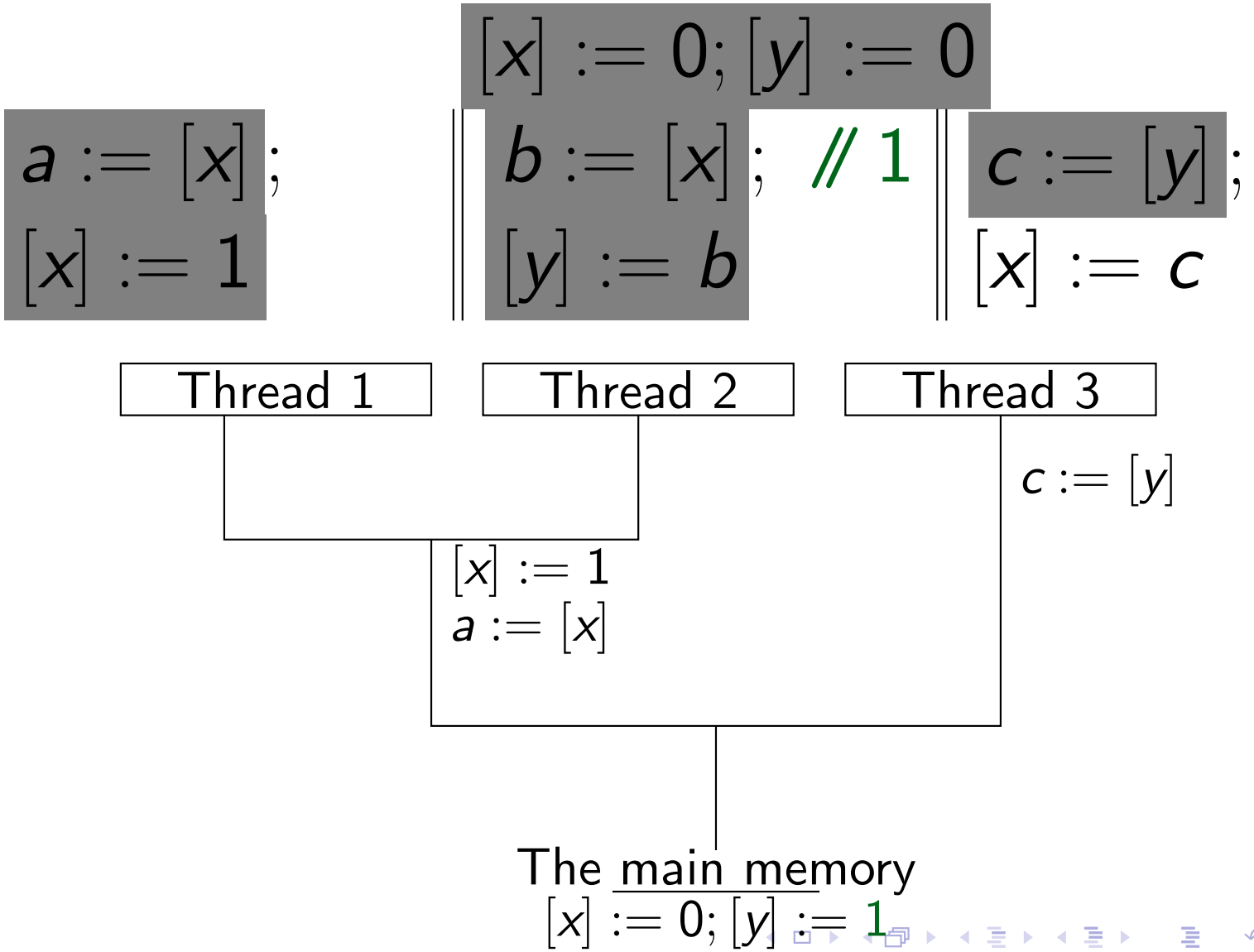
Example 3

$[x] := 0; [y] := 0$

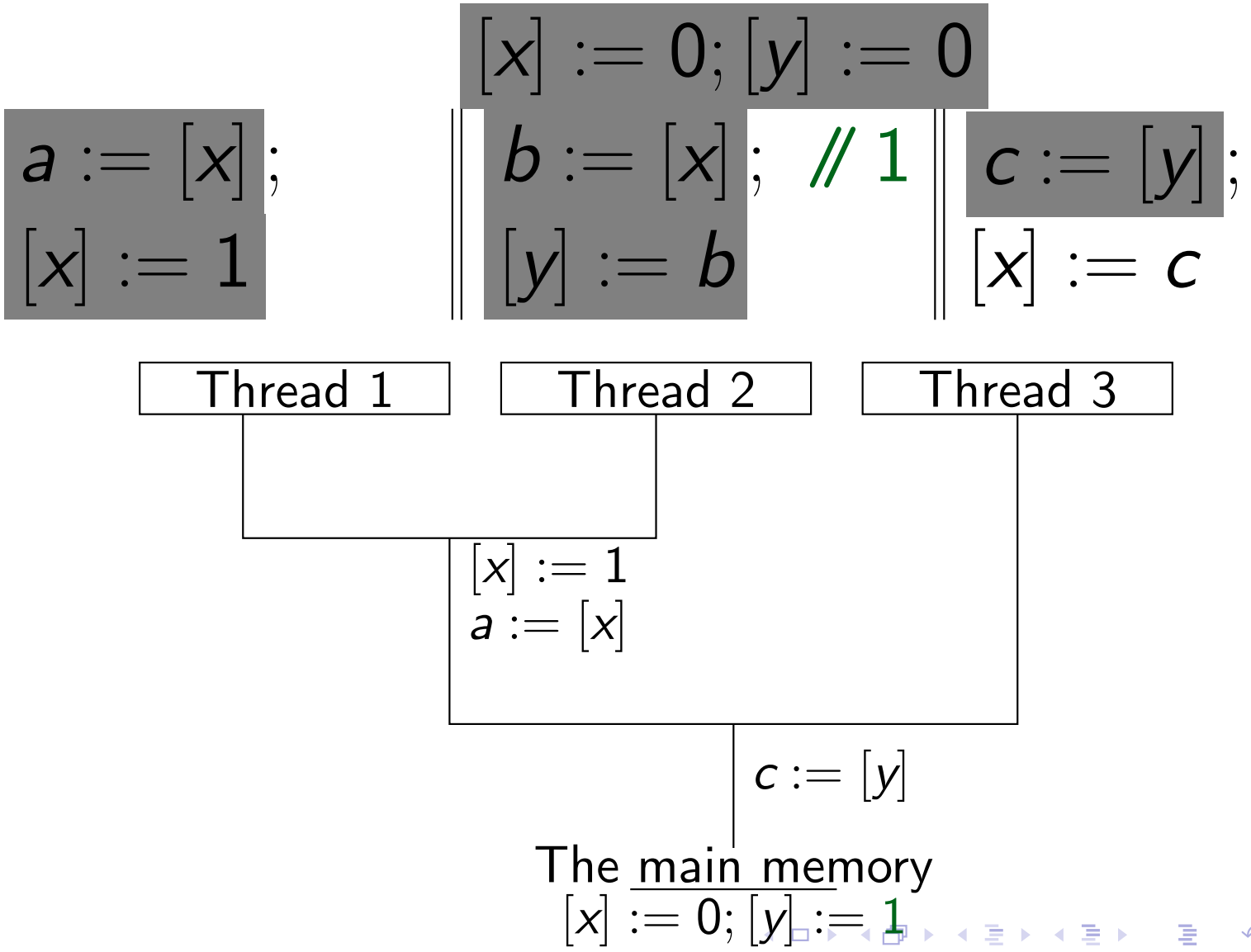
$a := [x]; \quad [x] := 1 \quad \| \quad b := [x]; \quad [y] := b \quad // 1 \quad \| \quad c := [y]; \quad [x] := c$



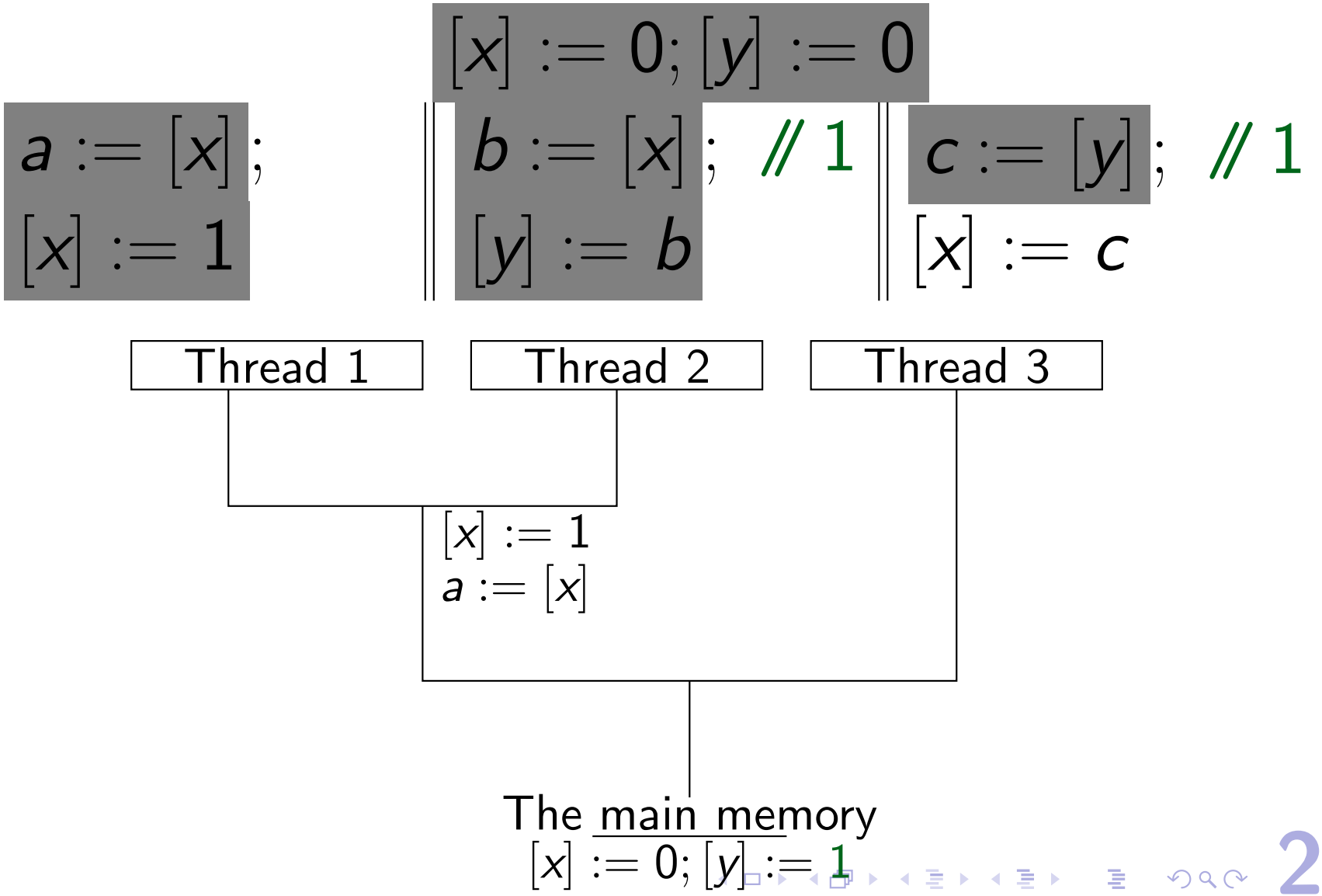
Example 3


[x] := 0; [y] := 0
a := [x];
[x] := 1
b := [x]; // 1
[y] := b
c := [y];
[x] := c
Thread 1
Thread 2
Thread 3
c := [y]
[x] := 1
a := [x]
The main memory
[x] := 0; [y] := 1

Example 3


[x] := 0; [y] := 0
a := [x];
[x] := 1
b := [x]; // 1
[y] := b
c := [y];
[x] := c
Thread 1
Thread 2
Thread 3
[x] := 1
a := [x]
c := [y]
The main memory
[x] := 0; [y] := 1

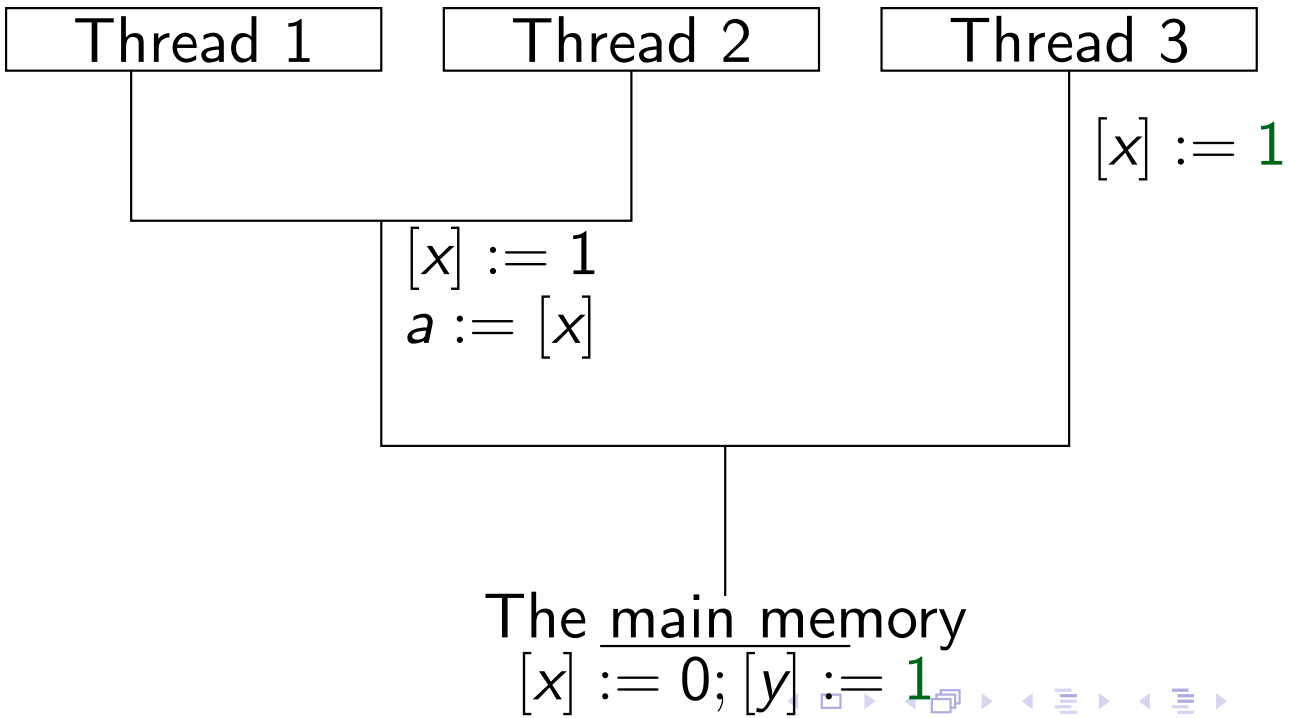
Example 3


[x] := 0; [y] := 0
a := [x]; [x] := 1
b := [x]; // 1 [y] := b
c := [y]; // 1 [x] := c
Thread 1
Thread 2
Thread 3
[x] := 1
a := [x]
The main memory
[x] := 0; [y] := 1

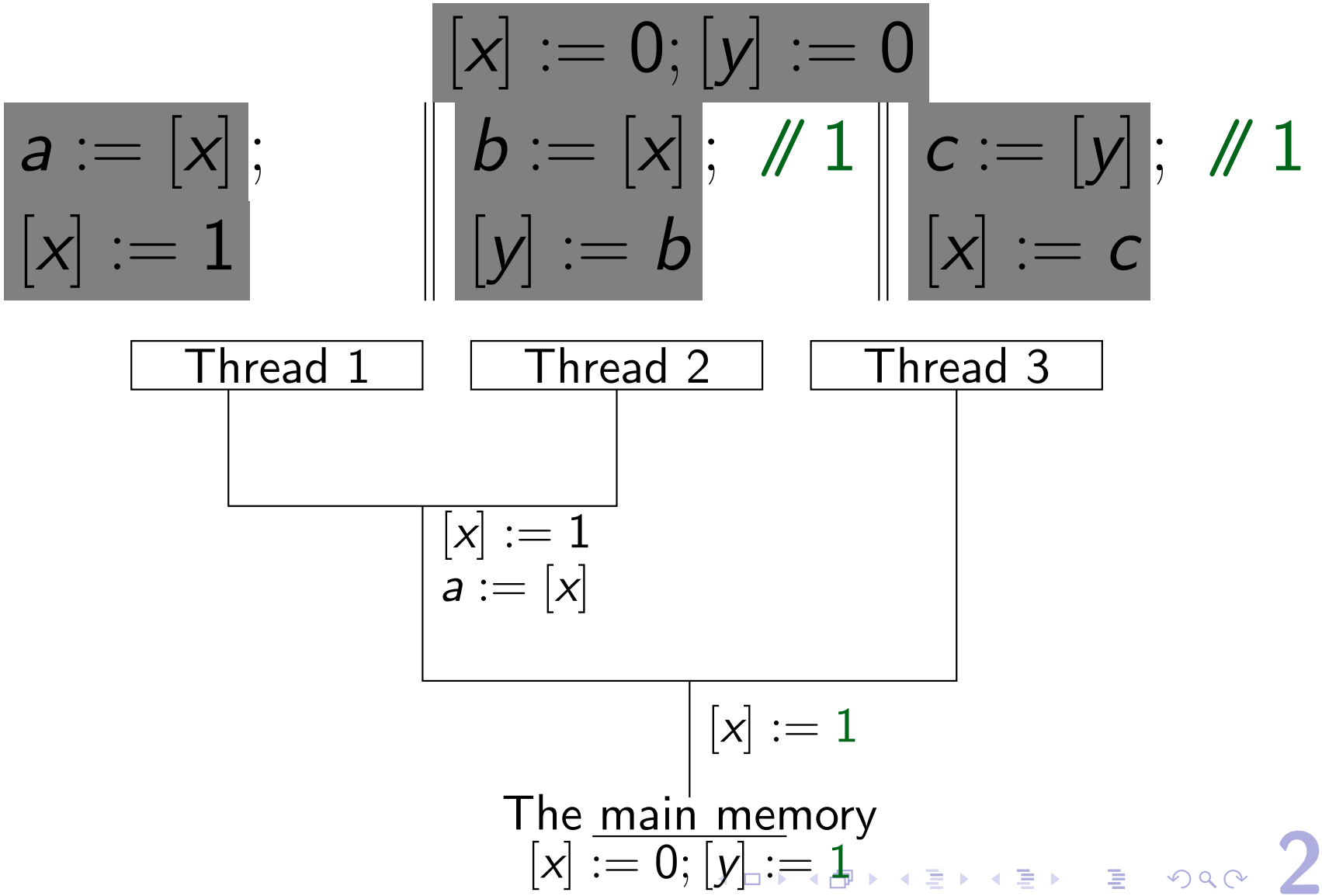
Example 3

$$[x] := 0; [y] := 0$$

$$a := [x]; \quad [x] := 1 \quad \| \quad b := [x]; \quad [y] := b \quad // 1 \quad \| \quad c := [y]; \quad [x] := c \quad // 1$$



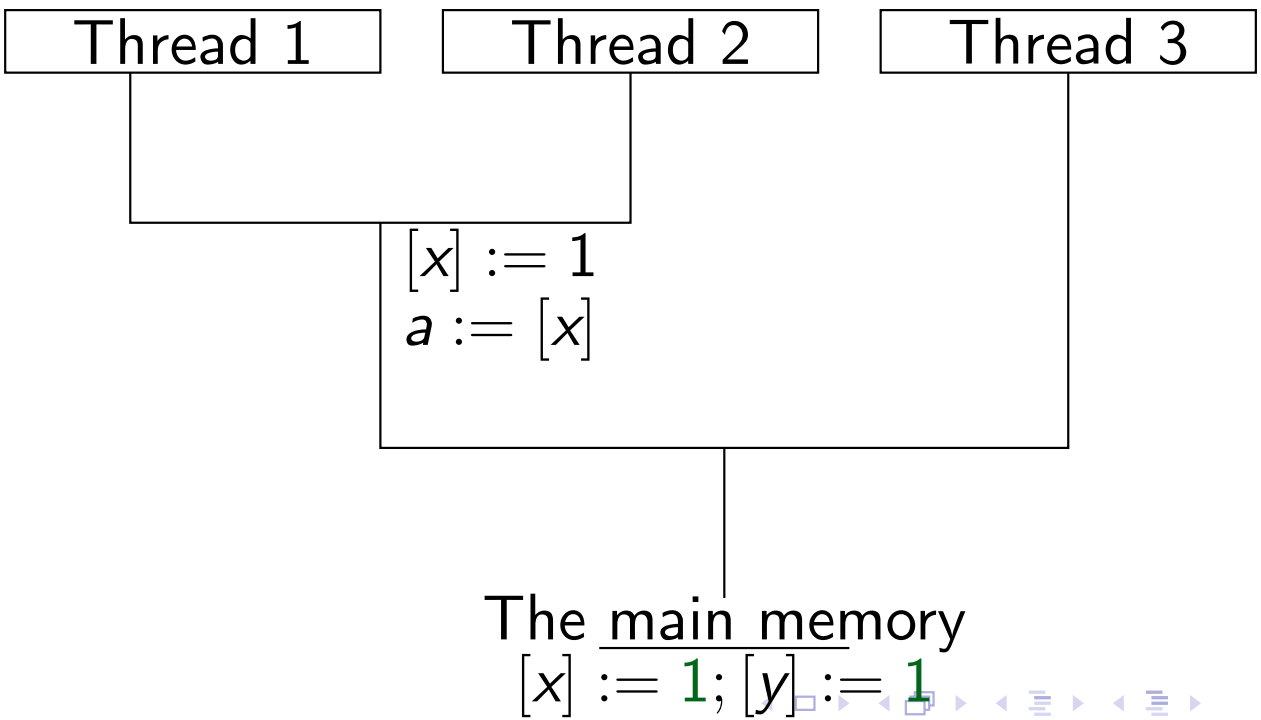
Example 3


[x] := 0; [y] := 0
a := [x]; [x] := 1
b := [x]; // 1
[y] := b
c := [y]; // 1
[x] := c
Thread 1
Thread 2
Thread 3
[x] := 1
a := [x]
[x] := 1
The main memory
[x] := 0; [y] := 1

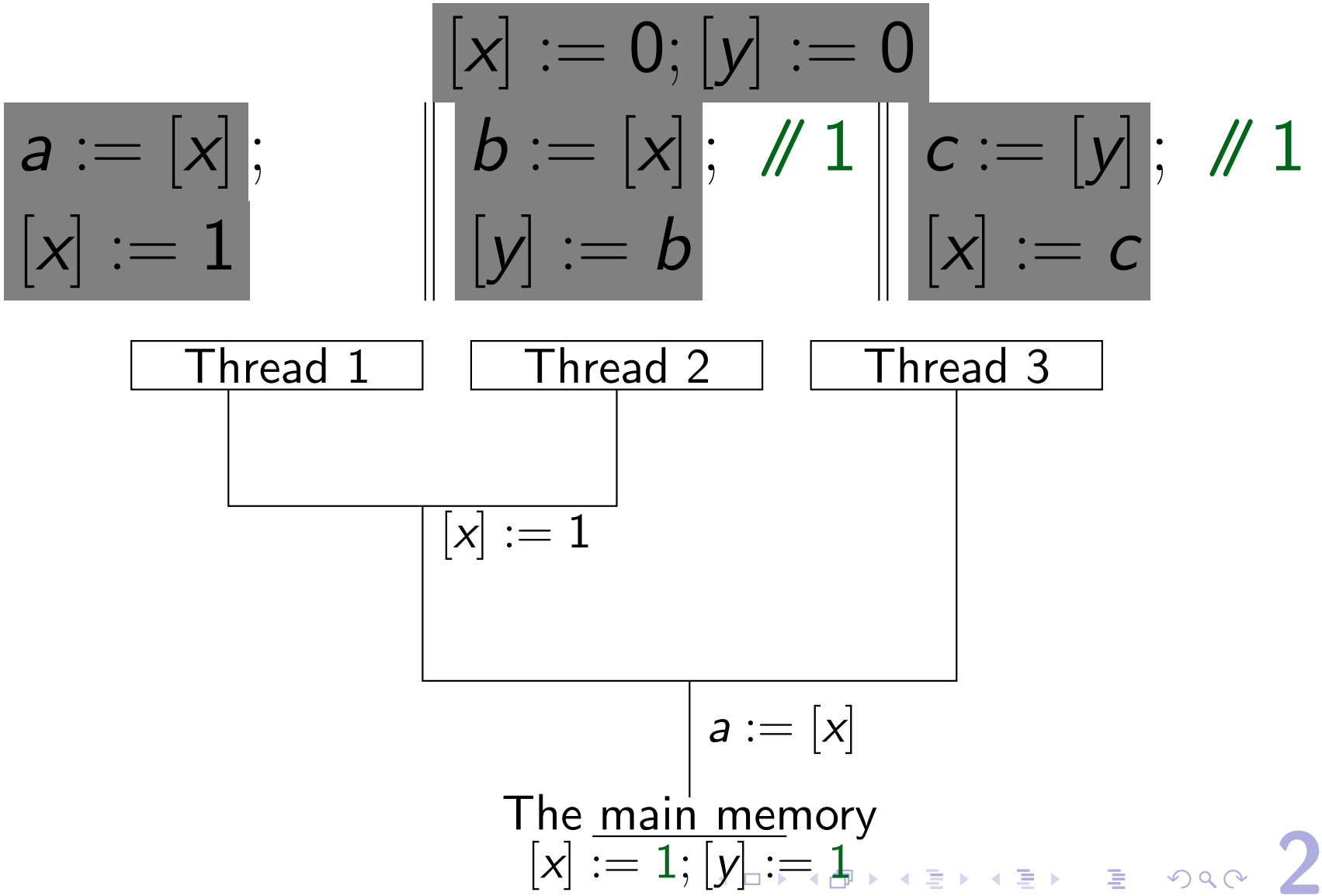
Example 3

$[x] := 0; [y] := 0$

$a := [x]; \quad [x] := 1 \quad \| \quad b := [x]; \quad [y] := b \quad // 1 \quad \| \quad c := [y]; \quad [x] := c \quad // 1$



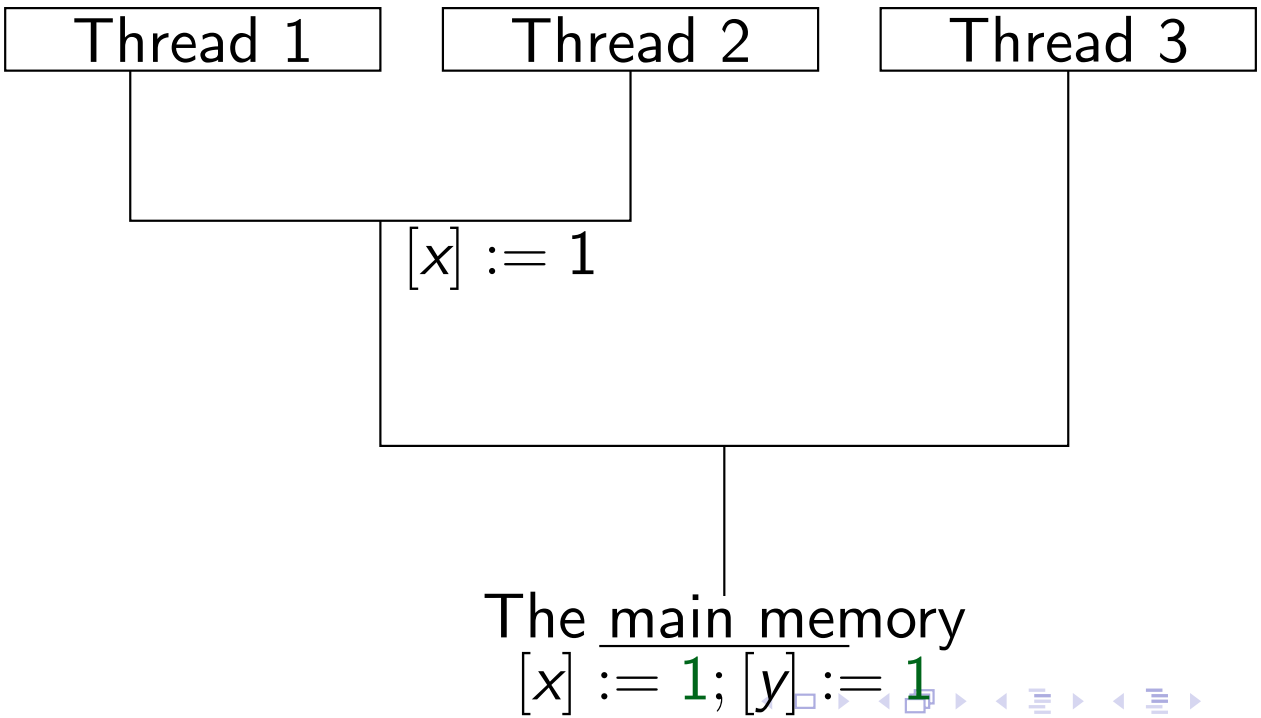
Example 3


[x] := 0; [y] := 0
a := [x]; [x] := 1
b := [x]; // 1 [y] := b
c := [y]; // 1 [x] := c
Thread 1
Thread 2
Thread 3
[x] := 1
a := [x]
The main memory
[x] := 1; [y] := 1

Example 3

$$[x] := 0; [y] := 0$$

$$a := [x]; \; // \, 1 \quad [x] := 1 \qquad \| \qquad b := [x]; \; // \, 1 \quad [y] := b \qquad \| \qquad c := [y]; \; // \, 1 \quad [x] := c$$

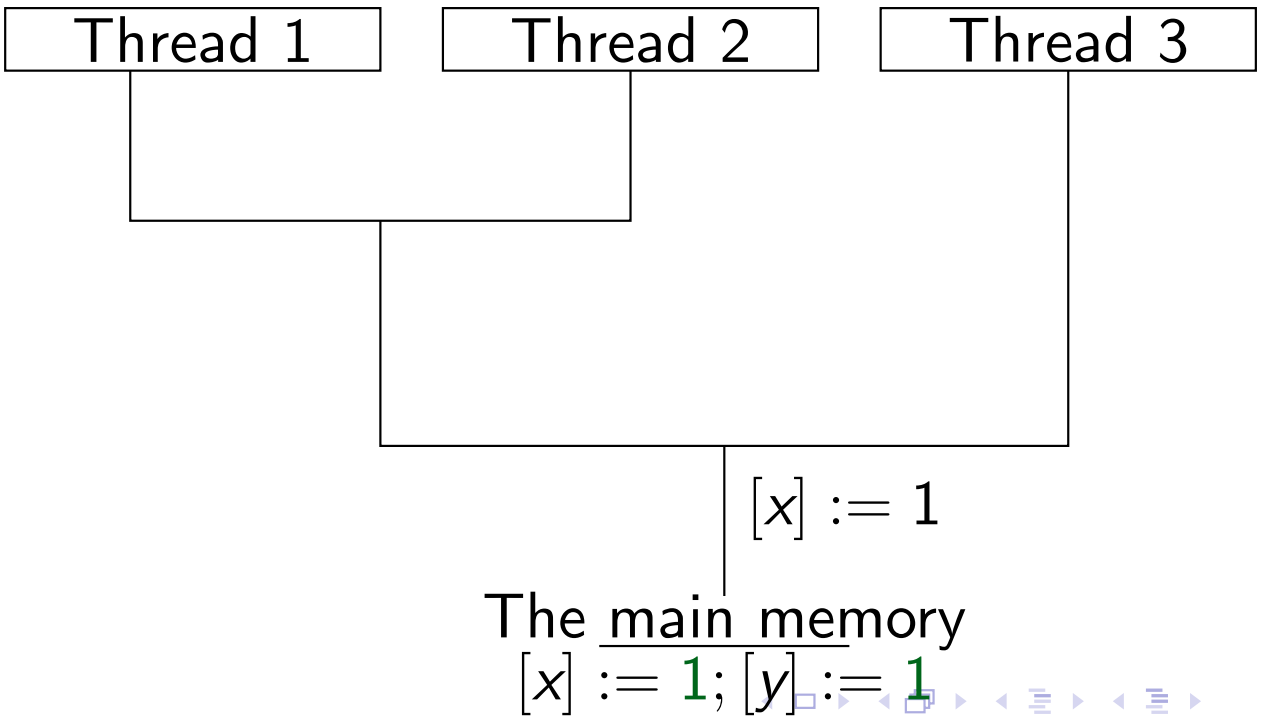


Example 3

$$[x] := 0; [y] := 0$$

$$a := [x]; \; // \; 1 \quad \| \quad b := [x]; \; // \; 1 \quad \| \quad c := [y]; \; // \; 1$$

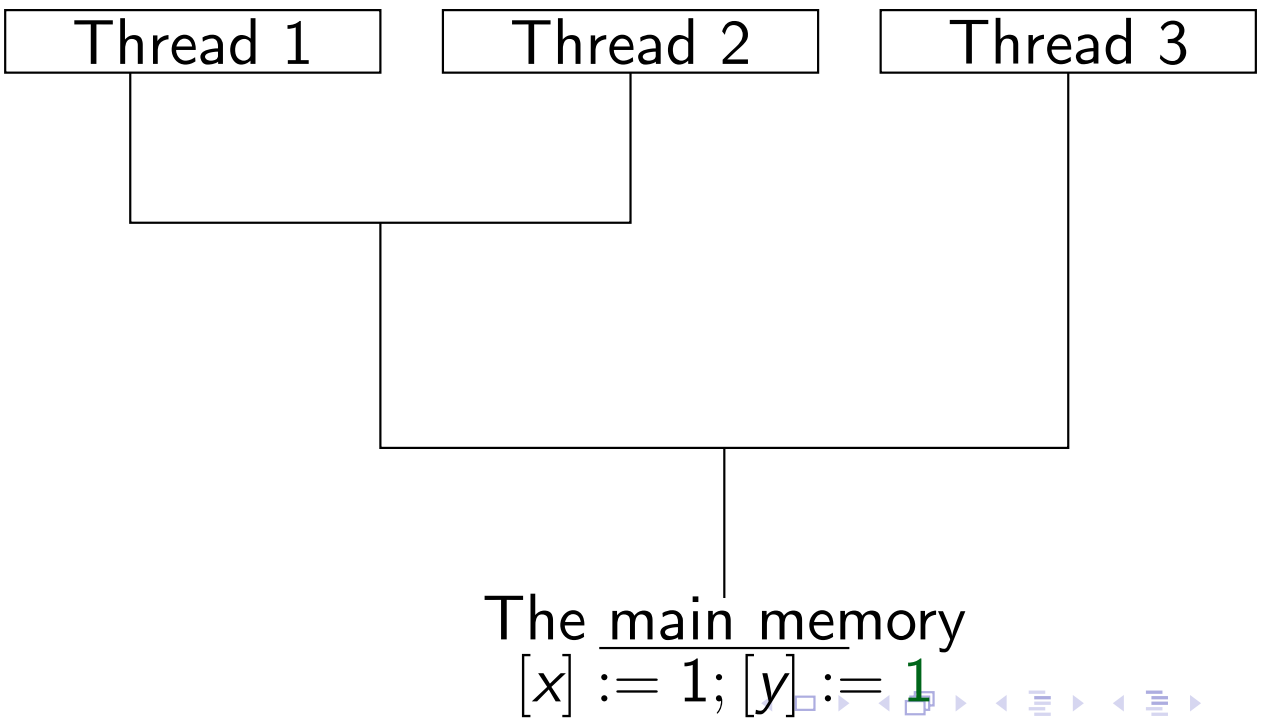
$$[x] := 1 \qquad\qquad [y] := b \qquad\qquad [x] := c$$



Example 3

$$[x] := 0; [y] := 0$$

$$\begin{array}{l} a := [x]; \\ [x] := 1 \end{array} \;\; /\!/ 1 \;\; \Big\| \;\; \begin{array}{l} b := [x]; \\ [y] := b \end{array} \;\; /\!/ 1 \;\; \Big\| \;\; \begin{array}{l} c := [y]; \\ [x] := c \end{array} \;\; /\!/ 1$$



Simulation

1. Introduce $SimInvariant : T_{State} \times S_{State}$;

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2. Show that

$$\forall t, t' \in T_{State}, s \in S_{State}.$$
$$correct(t), t \xrightarrow[T]{} t', SimInvariant(t, s),$$
$$\exists s' \in S_{State}. s \xrightarrow[S]{}^{*} s', SimInvariant(t', s').$$

The ARM+τ machine

- Add τ-map component to the ARM state;
- Modify **Write Commit** rule;
- Modify **Propagate** rule.

ARM+τ simulates ARM

$\forall Prog, \{\mathbf{s}_i\}_{i \in [0..n]}$,

ARM+τ simulates ARM

$$\forall \mathit{Prog}, \{\mathbf{s}_i\}_{i\in[0..n]},$$
$$\mathbf{s}^{\mathrm{init}}(\mathit{Prog}) = \mathbf{s}_0 \xrightarrow[\mathrm{ARM}]{} \ldots \xrightarrow[\mathrm{ARM}]{} \mathbf{s}_n, \mathsf{Final}^{\mathrm{ARM}}(\mathbf{s}_n),$$

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$$\exists \{\mathbf{a}_i | \mathbf{s}_i = \text{ARM}_{state}(\mathbf{a}_i)\}_{i\in[0..n]},$$
$$\mathbf{a}_0 \xrightarrow[\text{ARM}+\tau]{} \ldots \xrightarrow[\text{ARM}+\tau]{} \mathbf{a}_n.$$

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Sketch of the proof:

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$$\forall Prog, \{\mathbf{s}_i\}_{i\in[0..n]},$$
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$$\exists \{\mathbf{a}_i | \mathbf{s}_i = \text{ARM}_{state}(\mathbf{a}_i)\}_{i\in[0..n]},$$
$$\mathbf{a}_0 \xrightarrow[\text{ARM}+\tau]{} \ldots \xrightarrow[\text{ARM}+\tau]{} \mathbf{a}_n.$$

Sketch of the proof:

- Construct an order on writes from $\mathbf{s}_n$;
- Show $\mathbf{s}_i$ doesn't contradict the order for all i;
- Show the order may coincide with τs in $\{\mathbf{a}_i\}_{i\in[0..n]}$.